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Engineering Guidelines for High-Speed Loadboard Design

Electrical Characterization
0.05 - 10.05 GHz

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Summary

Objective:
This document should be used as a design guideline to maximize the bandwidth of loadboards using Aries Electronics' High-Performance RF Test Sockets.

Methodology:
This design guideline is based on measurements taken on Aries sockets over the past few years and design experience gained by GigaTest Labs in the process of developing high-speed loadboards for use in RF production testing.

All measurements were performed using a high-frequency test system. This consists of the HP8510C network analyzer, MicroCoax 40 GHz 2.92mm (K-conn) coaxial cables, GGB 450μm Picoprobes and GigaTest Labs 4040 probe station. In all cases the measurement system was calibrated using the SOLT (short-open-load-thru) calibration.

All modeling was performed under Hewlett-Packard's Microwave Design System.

Design procedure:
The design procedure to follow is:
1. Define the package pitch.
2. Find the recommended board stack-up and predicted performance.
3. Layout the socket footprint per Aries specifications.
4. Perform ground and power connections as specified on page **iv**.
5. Perform high-speed signal connections as specified on page **v**.
6. Find predicted SPICE model on page **vii-viii**.

Define Package Pitch
The correct package pitch is called out on the Aries' footprint drawing that is supplied with every socket order.

Recommended board stack-up
The main parameter in the design process is the spacing between the Aries socket and the ground plane immediately below. Figure 1 shows a cross-section of an Aries socket mounted onto a PCB. The socket contacts rest directly on top of gold-plated

pads on the surface of the PCB. To achieve the best performance possible, for a given package pitch, spacing "h" to the ground plane should be setup as defined in table 1. This insures the best impedance match to 50 Ω and contact-to-contact isolation.

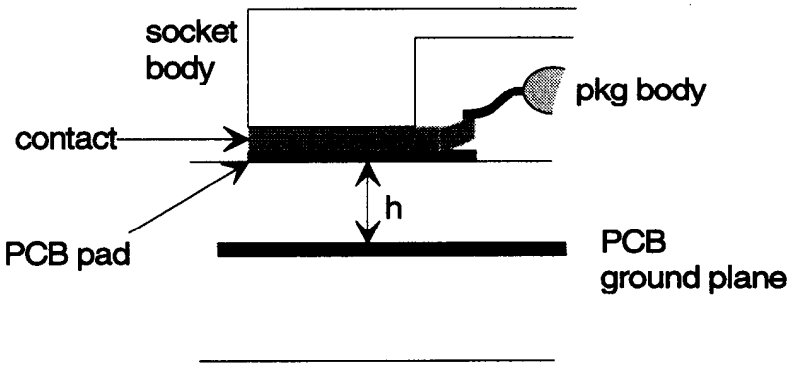


Figure 1 - Aries socket in loadboard environment

Table 1: Recommended loadboard stack-up & predicted performance

Pkg. Pitch	h (in)	isolation up to 10 GHz (dB)	bandwidth (1dB loss)
2.54mm	.030"	> 17 dB[4]	> 10 GHz[4]
1.27 mm	.015"	> 17 dB[1, 3]	> 10 GHz[3]
0.8 mm	.009"	> 17 dB[1, 3]	> 10 GHz[3]
0.65 mm	.007"	> 17 dB[1, 3]	> 10 GHz[3]
0.5 mm	.007"	> 14 dB[2, 3]	8 GHz[3]

[1] 17dB isolation is equivalent to 14% voltage crosstalk

[2] 14dB isolation is equivalent to 20% voltage crosstalk

[3] Measured performance

[4] Simulated performance

Power and ground connections:

1. Connect the power and grounds on the inside and outside perimeters of the socket footprint using the largest diameter vias possible. All planes on the same net should be connected together.
2. Place vias as close as possible to the contact pads, without violating the contact pad geometry specification. This insures minimum inductance in the power and ground connections.

3. Use two or more vias in parallel where possible to reduce the inductance.
4. For adjacent pins on the same net, the pads should be shorted together to reduce the overall inductance.

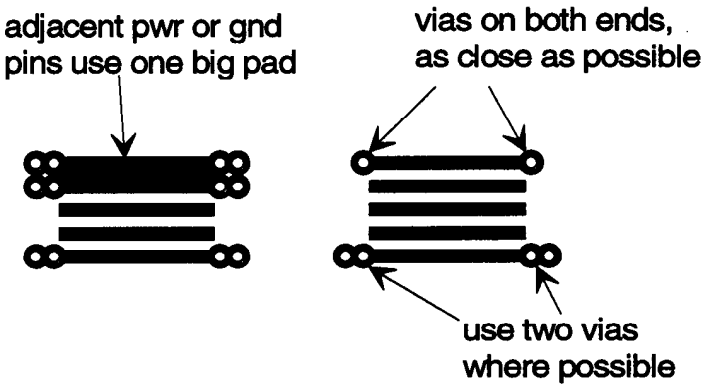


Figure 2 - Power and ground connections

High-speed signal connections:

The signal connections must be done with the minimum parasitics. Four cases are investigated:

1. Microstrip on same side as socket: adjust linewidth from 50 Ω to the contact width specified by Aries.

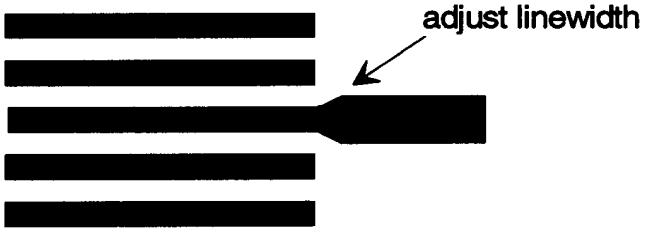


Figure 3 - Same-side microstrip connection

2. Microstrip on opposite side of socket: place .010" via transition as close as possible to socket. Connect top and bottom ground planes with vias.

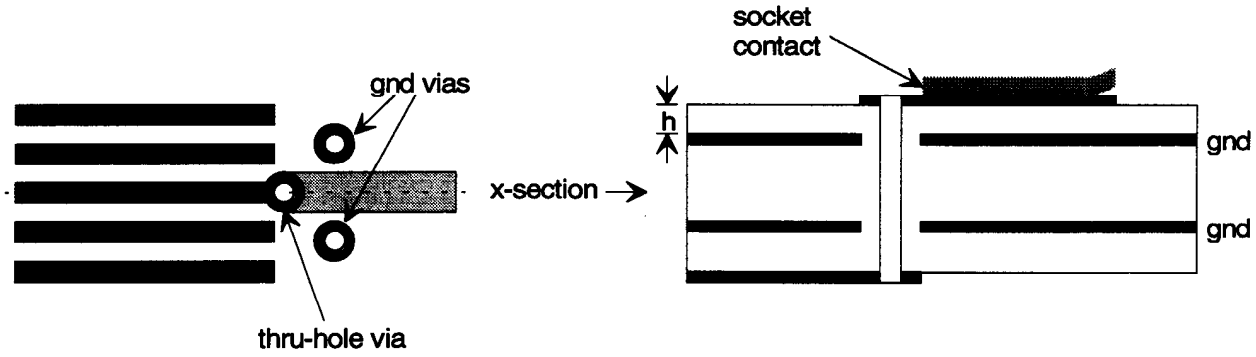


Figure 4 - Opposite-side microstrip connection

3. Stripline on same side as socket: place 10-mil **blind** via transition as close as possible to socket and relieve the ground plane below the via. Do not use a thru-hole to make the connection, since the via-stub capacitive parasitics will degrade the performance. In .125" boards this parasitic can account for up to 50% bandwidth reduction.

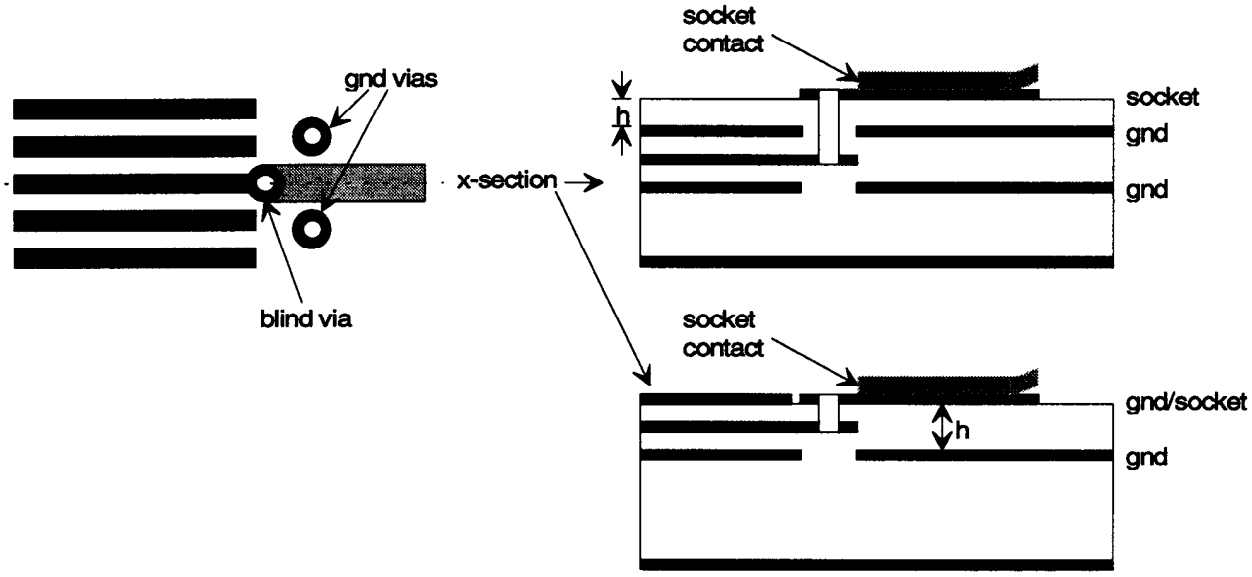


Figure 5 - Same-side stripline connection

4. Stripline on opposite side of socket: place .010" thru-hole via as close as possible to socket, use the minimum pad possible. A via stub greater than 12 mils is not recommended because of its parasitics. Ideally a blind via would be used in this case as shown in figure 5.

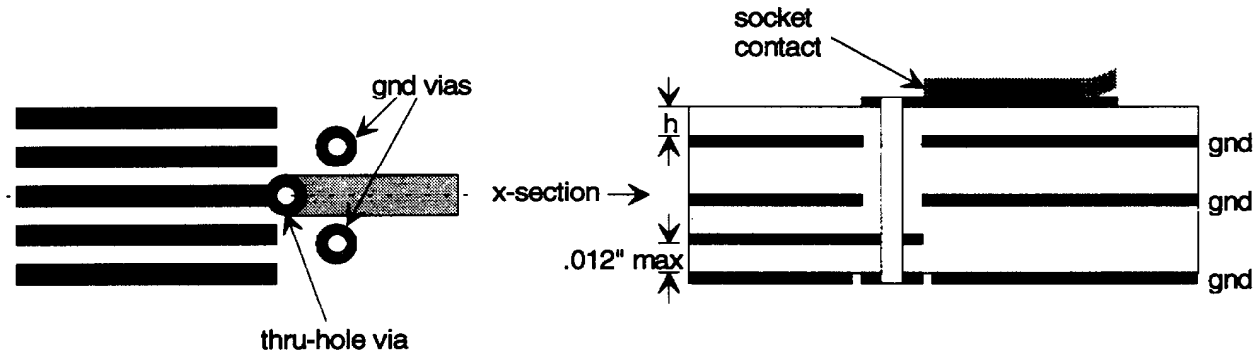


Figure 6 - Opposite-side stripline connection

Special considerations:

1. Packages with metal bodies & ground slugs should use the star-contact option offered by Aries. This configuration allows to ground the packages with very low inductance (0.035 nH). The measured ground-bounce versus frequency can be found in the appendix page 1.
2. If greater pin-to-pin isolation is needed, use grounded contacts. Each grounded contact will improve the isolation by 10 dB.

SPICE-compatible models:

The equivalent-circuit topology is shown in figure 7.

Element definitions:

L_1 & L_2:	self-inductance of one socket pin
R_1 & R_2:	resistors in parallel with L_1 & L_2 used to model high-frequency losses like skin-effect and loss tangent
C_{1a} & C_{2a}:	capacitance to ground of one socket pin (PCB side)
C_{1b} & C_{2b}:	capacitance to ground of one socket pin (package side)
M_{21}:	mutual-inductance between adjacent socket pins
C_{21a}:	mutual-capacitance between adjacent socket pins (PCB side)
C_{21b}:	mutual-capacitance between adjacent socket pins (package side)

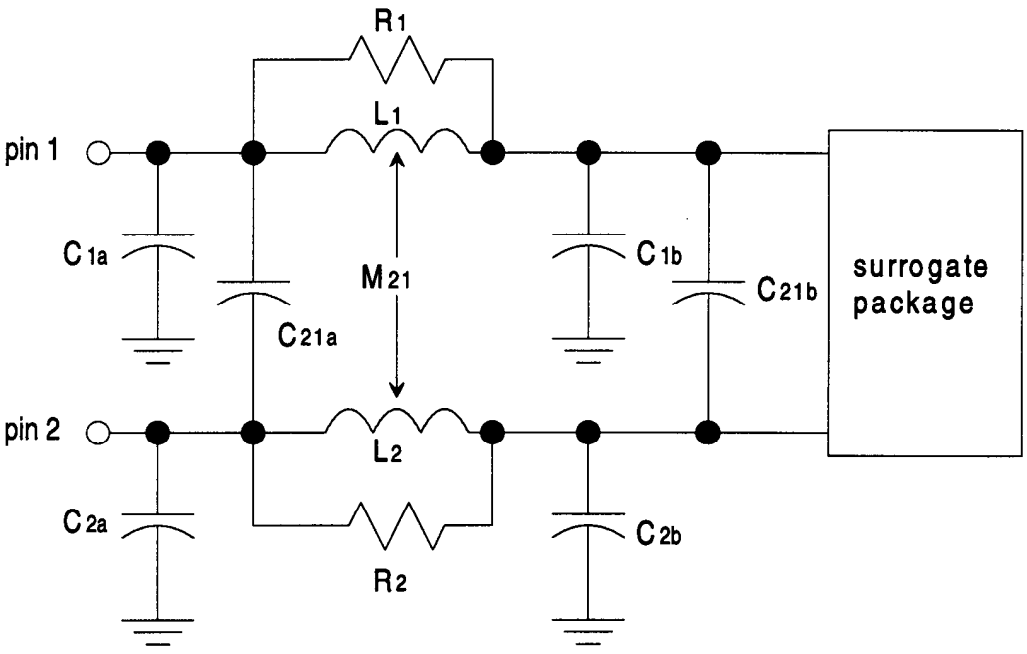


Figure 7 - Equivalent-circuit model

Element values:

Table 3 shows the element values for the different socket pitches. The model bandwidth is DC to 5.05 GHz, which will easily handle signal with risetimes of 200 ps or greater.

Table 2: Element values

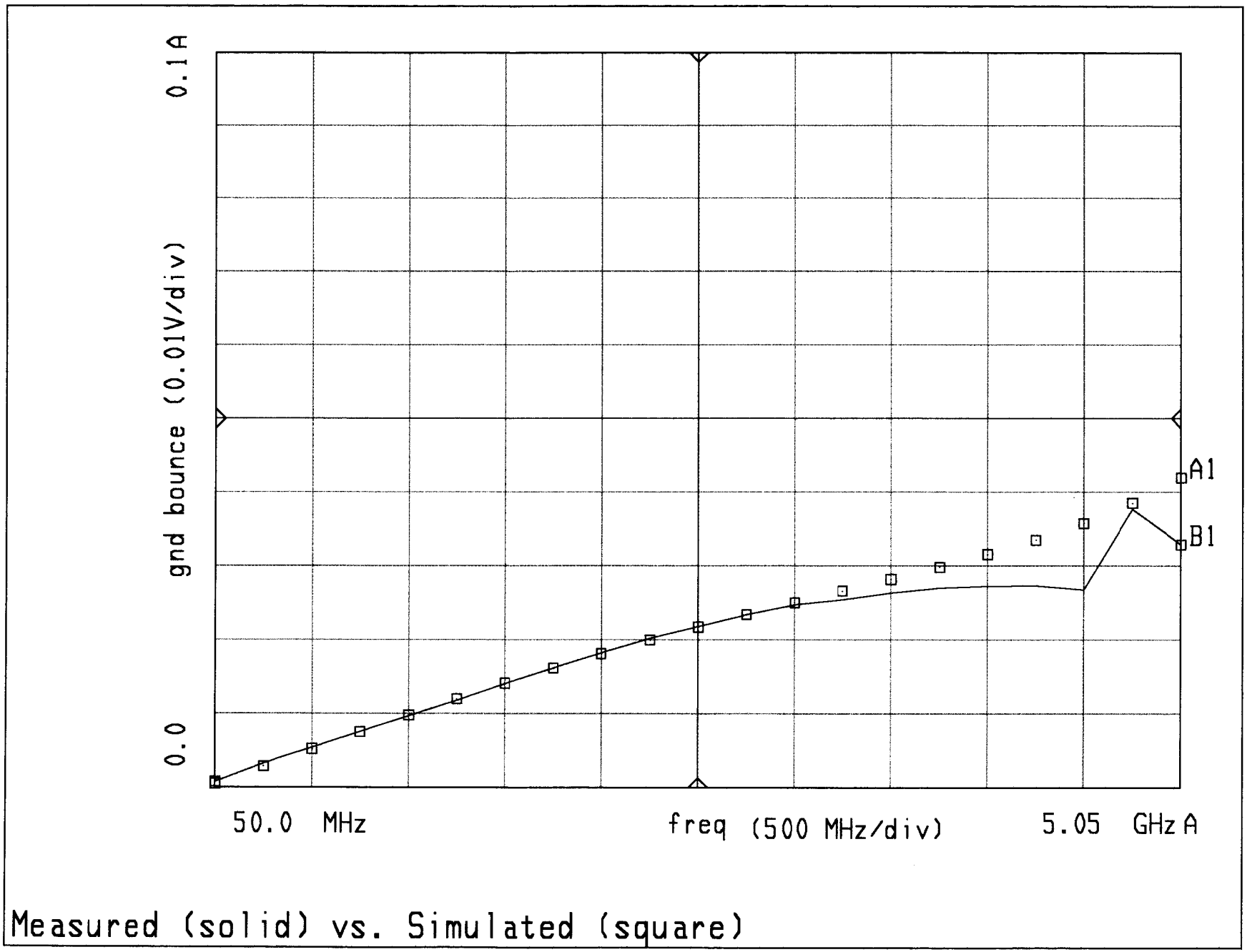
socket pitch	L_1 & L_2 (nH)	M_{21} (nH)	R_1 & R_2 (Ω)	C_{1a} & C_{2a} (pF)	C_{1b} & C_{2b} (pF)	C_{21a} (pF)	C_{21b} (pF)
0.5mm	1.35[1]	0.30	600	0.35	0.40	0.08	0.09
0.65mm	1.35[1]	0.20	750	0.35	0.45	0.04	0.05
0.8mm	1.50[1]	0.25	1000	0.30	0.35	0.05	0.06
1.27mm	1.50[1]	0.25	1000	0.30	0.35	0.05	0.06

[1] For power and ground pins with vias on the inside perimeter the self-inductance to those vias is 0.2nH.

Appendix

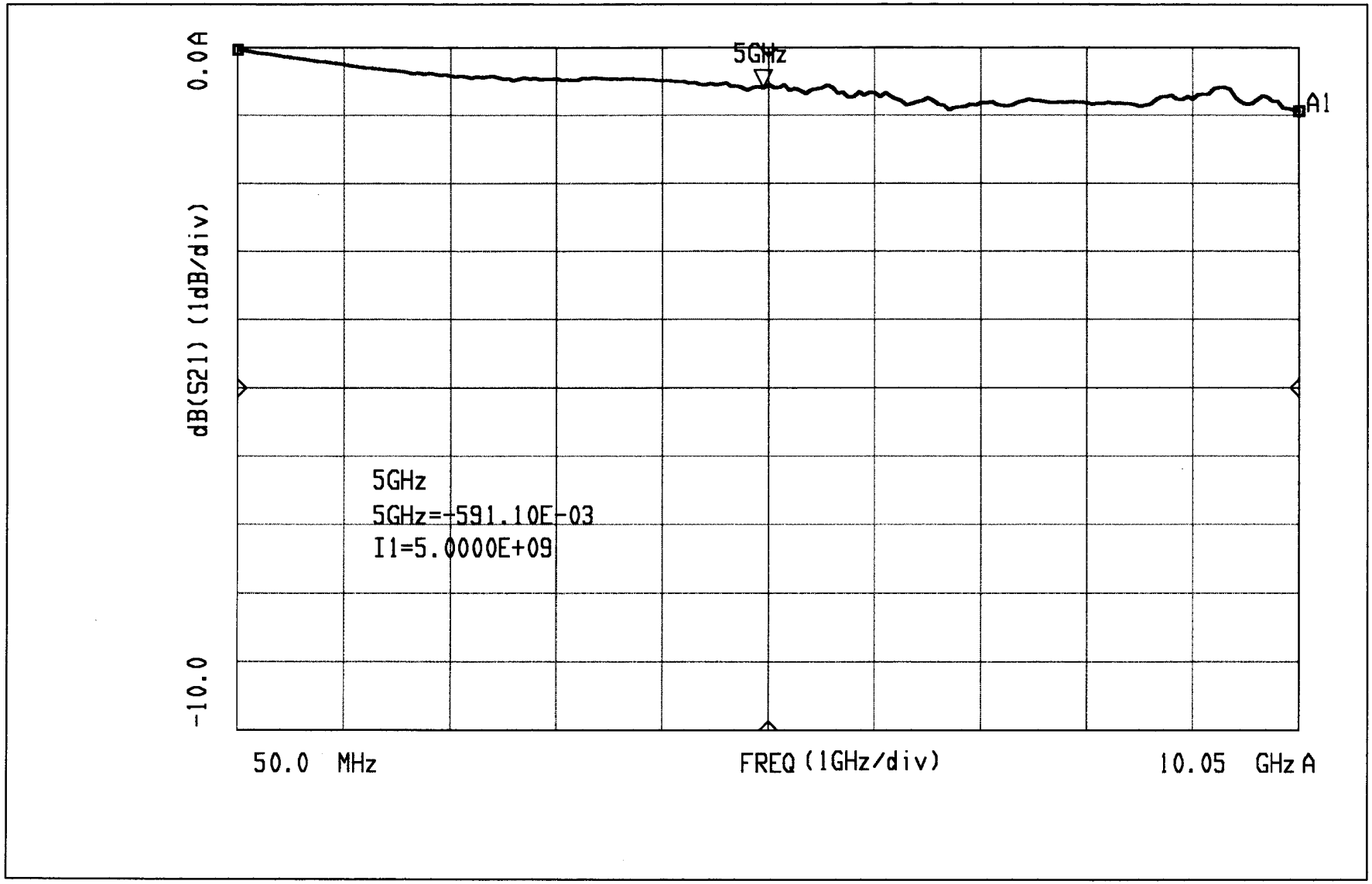
The following section shows selected data from the measurements and simulations performed.

Star-Contact Ground-Bounce Performance



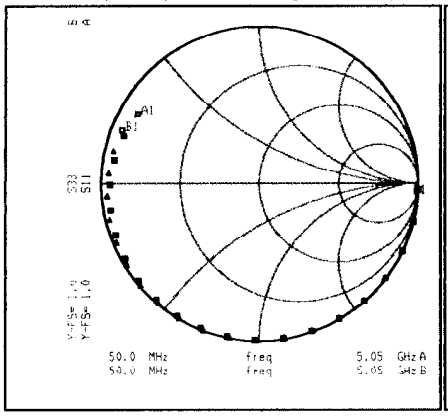
Measured (solid) vs. Simulated (square)

Aries Electronics Socket (0.65mm pitch) - Loss vs. Freq

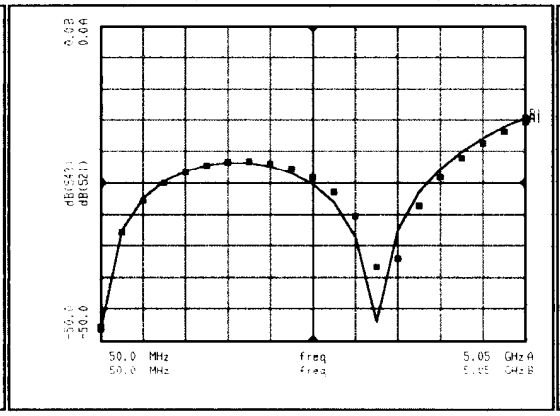


Aries Socket (0.65mm) - Open measurement

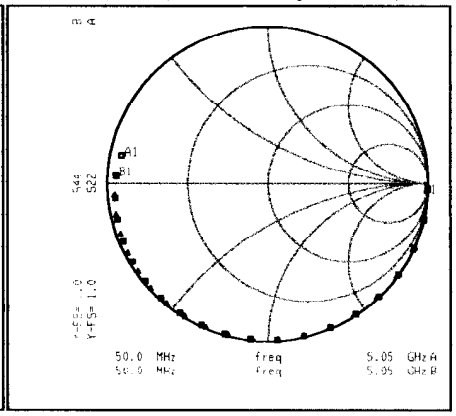
Reflection response of pin 3 - meas (triangle) vs sim (square)



Crosstalk between pins 3 & 4 - meas (solid) vs sim (square)

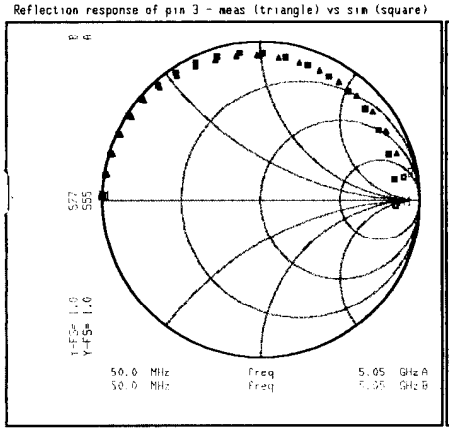


Reflection response of pin 4 - meas (triangle) vs sim (square)

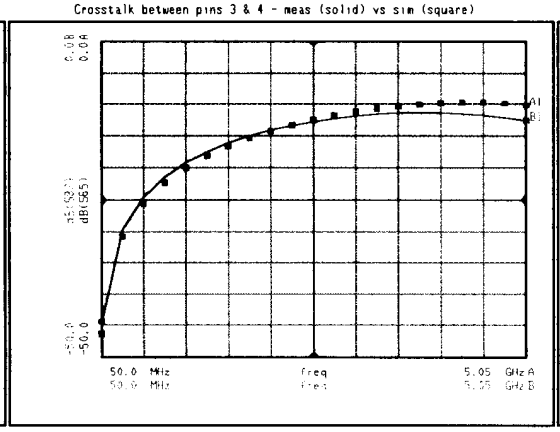


Aries Socket (0.65mm) - Shorted Measurement

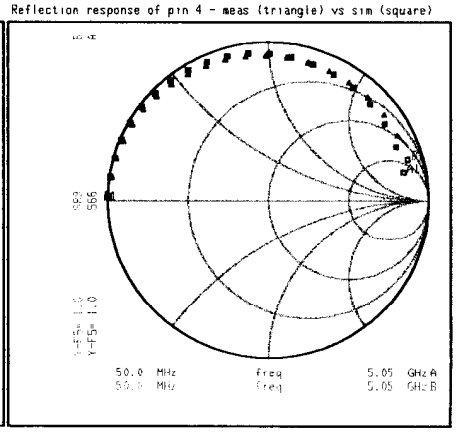
Reflection response of pin 3 - meas (triangle) vs sim (square)



Crosstalk between pins 3 & 4 - meas (solid) vs sim (square)

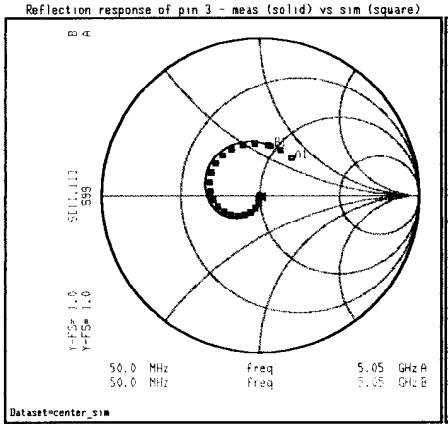


Reflection response of pin 4 - meas (triangle) vs sim (square)

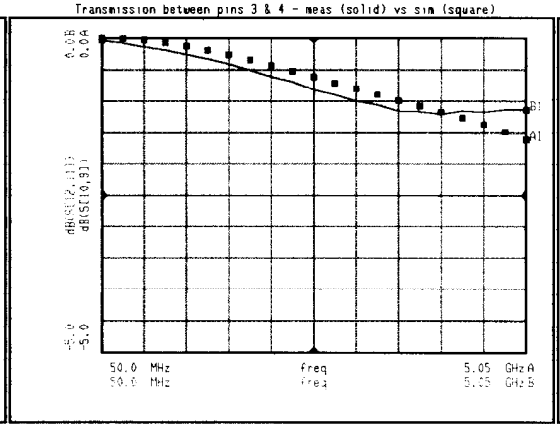


Aries Socket (0.65mm) - Thru Measurement

Reflection response of pin 3 - meas (solid) vs sim (square)



Transmission between pins 3 & 4 - meas (solid) vs sim (square)



Reflection response of pin 4 - meas (solid) vs sim (square)