Aries
CSP microstrip socket
Cycling test

RF Measurement Results

prepared by

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2/18/05

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Table of Contents

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Objective

The objective of these measurements is to determine the changes in RF performance of an Aries CSP microstrip socket as it is subjected to a cycling regimen. The measurements are performed as in the individual characterization, i.e. for G-S-G configurations, a signal pin surrounded by grounded pins is selected for the signal transmission. For G-S-S-G configurations, two adjacent pins are used to transmit signals. All other pins are grounded. Measurements in both frequency and time domain form the basis for the evaluation. Parameters to be determined are pin capacitance and inductance of the signal pin, the propagation delay, and the attenuation to 40 GHz.

Methodology

Cycling of the sockets is performed according to a prescribed binary sequence. A socket is characterized after 0, 8192, 65536, 262144 and 1048576 insertions of a surrogate device. After each sequence, the surrogate device is exchanged. This means that a surrogate device may be inserted repeatedly for a large number of cycles, especially later in the test. While not entirely corresponding to an actual test situation, this approach minimizes the number of surrogate devices required and does not depend on the construction and availability of any specialized handlers.

Capacitance and inductance for the equivalent circuits were determined through a combination of measurements in time and frequency domain. Frequency domain measurements were acquired with a network analyzer (HP8722C). The instrument was calibrated up to the end of the 0.022" diameter coax probe. The probe was then connected to the fixture and the response measured from one side of the array. When the pins terminate in an open circuit, a capacitance measurement results. When a short circuit compression plate is used, inductance can be determined.

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Time domain measurements are obtained via Fourier transform from VNA tests. These measurements reveal the type of discontinuities at the interfaces plus contacts and establish bounds for digital system risetime and clock speeds.

The focus of this test was stability and repeatability. Deviations from the actual characterization of the device as reported in the cycle 0 test reports may therefore be apparent. This was tolerated in the interest of interchangeability and uniformity of testing since the test setup and procedures were simultaneously used for a number of different sockets.

A number of points are unique to testing of a socket with a microstripline connection. The first issue is that of calibration. Open circuit and short circuit measurements are calibrated to the end of the microstripline in the test fixture. Any changes of the line properties will have an immediate adverse effect on the measurement accuracy. Such changes are brought about by inserting the socket into the mounting plate. When that happens, the dielectric material of the socket (around its contactor) alters the characteristic impedance of the entire line, and therefore the calibration.

Parasitic transmission lines are a second issue. The physical arrangement of the socket allows for creation of short- (or open-) circuited stubs of metal over ground or metal:
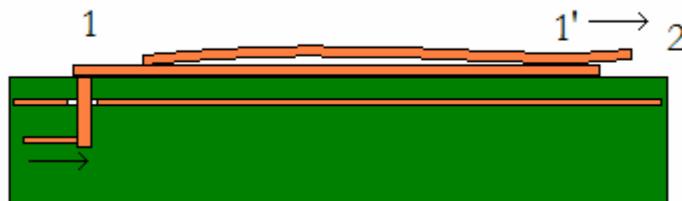
Such a situation can exist between points 1 and 1', for example. This creates a low loss transmission line that will be closely coupled to the microstripline on the PCB. This situation can also exist on the ground connections adjacent to the microstripline itself.

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Careful assembly and during cycle0 testing prevented this from occurring. As will be seen, in the cycling test setup it was not possible to always prevent this.

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Test procedures

To establish capacitance of the signal pin with respect to the rest of the array, a return loss calibration is performed. Phase angle information for S11 is selected and displayed. When the array is connected, a change of phase angle with frequency can be observed. It is recorded and will be used for determining the pin capacitance.

The self-inductance of a pin is found in the same way, except the CSP microstrip socket contact array is compressed by a metal plate instead of an insulator. Thus a short circuit at the far end of the pin array results. Again, the analyzer is calibrated and S11 is recorded. The inductance of the connection can be derived from this measurement.

Setup

The setup used for the cycling consists of a small mechanical device with two parallel plates (see Fig.1). The plate spacing of this cycler varies periodically and is adjustable to a rate of up to 3 cps. Overdrive conditions are adjusted with shims according to the requirements of the individual socket. A presettable counter controls the number of test cycles. For the parallel plate setup force limiting was accomplished by inserting a thin hard rubber sheet between the DUT and the moving plates. Parameters were selected such that under maximum deflection and normal cycling conditions the surrogate device touches the bottom of the socket. Where necessary, pressure sensitive paper was used to verify this condition.

When a solenoid based cycler was used (typically after 64k cycles), force limiting was via solenoid drive current when necessary. Force measurements were performed with a pressure indicating paper that is capable of determining the magnitude of the

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applied pressure and hence the force. This method is necessary because of the dynamic situation that exists with the solenoid plunger / surrogate chip holder assembly entering the socket with some speed and hence contributing to the maximum force. Maximum operating speed was 10 cycles per second.

Figure 1 Socket cycling station

Testing was performed with a test setup that consists of a brass plate that contains the coaxial probes. The socket is aligned and mounted to that plate. The opposite termination is also a metal plate with coaxial probes, albeit in the physical shape of an actual device to be tested.   Fig. 2 shows a typical arrangement of base plate and DUT probe:
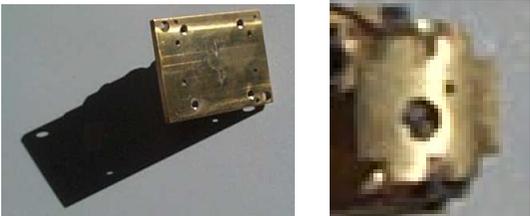
Figure 2 Socket mounting plate and DUT test plate

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For cycling, the socket is mounted on a brass plate with Au over Ni coating equivalent to that found on PCBs. This plate also provides for insertion of a DC test probe for DC measurements.

After the prerequisite number of surrogate device insertions, the socket is transferred to the RF test base plate for characterization. The CSP microstrip socket and base plate as well as the DUT plate are then mounted in a test fixture as shown below in Fig. 3:
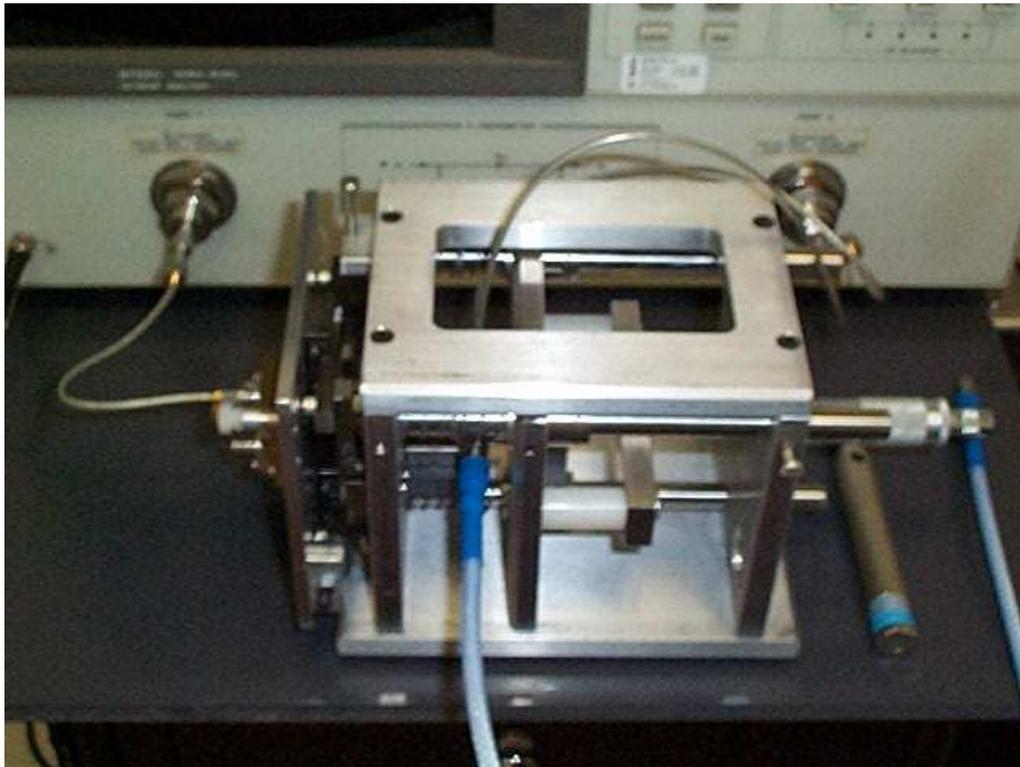
Figure 3 Test fixture

This fixture provides for independent X, Y and Z control of the components relative to each other. X, Y and angular alignment is established once at the beginning of a test series and then kept constant. Z alignment is measured via micrometer and is established according to specifications for the particular socket. Connections to the VNA are made with high quality coaxial cables with K connectors.

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After RF characterization, the socket is transferred back to the dc test plate for further cycling.

For G-S-S-G measurements, the ports are named as follows:
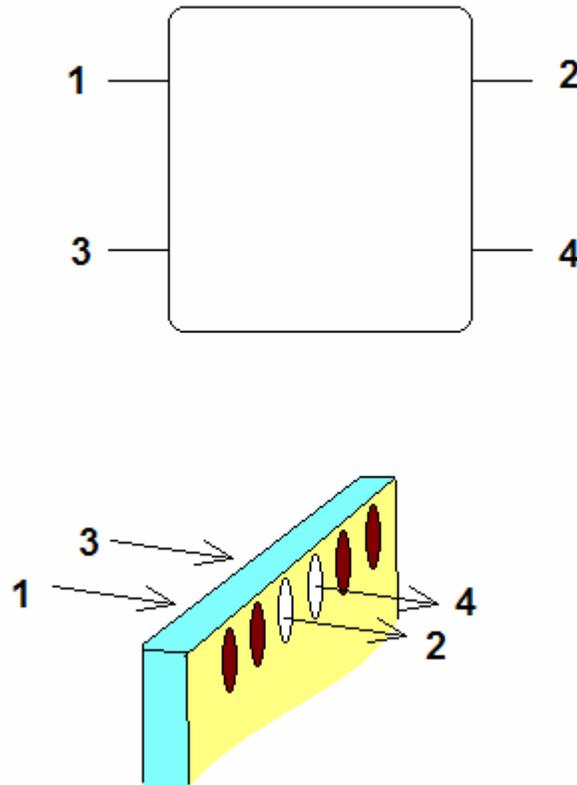
Figure 4 Ports for the G-S-S-G measurements

Signals are routed though two adjacent connections (light areas), unused connections are grounded (dark areas).

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It should be noted that the port naming convention used here deviates from the traditional port assignments to be compatible with the existing data acquisition software.

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Measurements G-S-G

Time domain

The time domain measurements will be presented first because of their significance for digital signal integrity. TDR reflection measurements (and the corresponding color key) are shown in the following graphs:
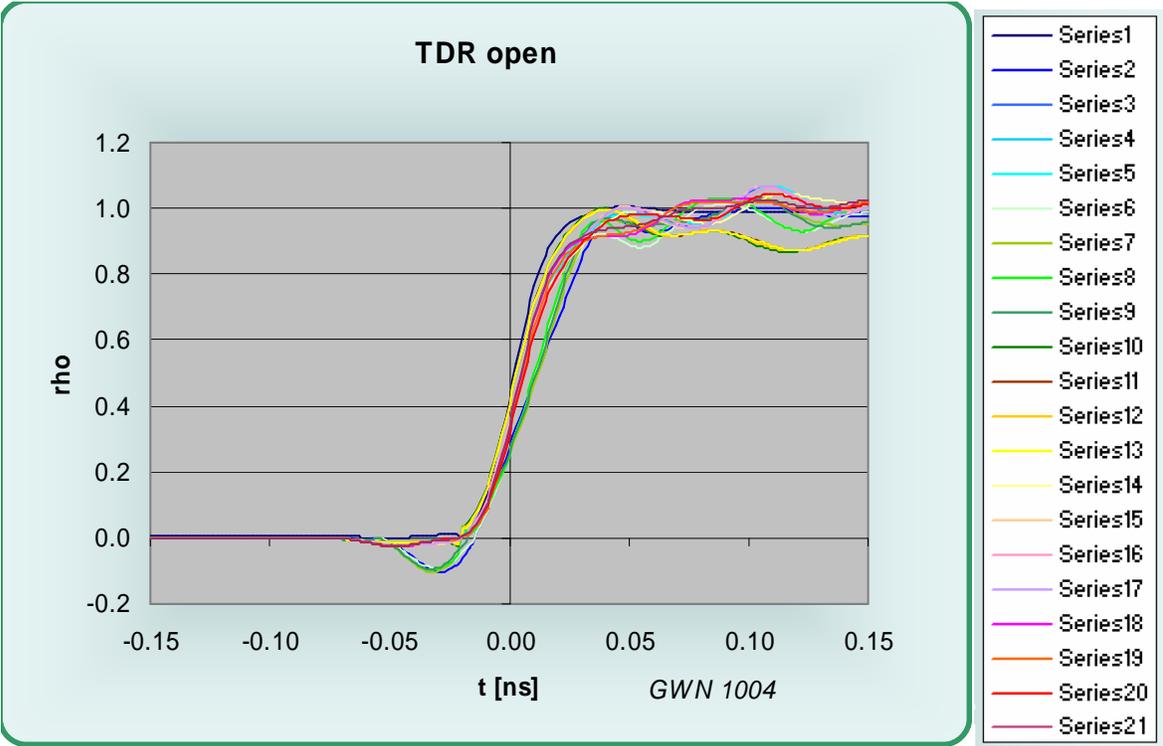
Figure 5 TDR signal from an OPEN circuited CSP microstrip socket

The reflected signals from the CSP microstrip socket (rightmost traces) show only a small deviation in shape from the original waveform (leftmost trace). The average risetime is 37.8 ps and is only slightly larger than that of the system with the open probe (28.5 ps). The risetime standard deviation is 5.3 ps throughout the sequence of tests.

Average electrical pin length is 1.9 ps one way with a standard deviation of 1.5 ps.

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Statistical data was extracted from the datasets at each particular point in time.

Deviations as a function of time

Legend: VARP, STDEV, AVEDEV, DEVSQ, SKEW, DEVMAX, DEVMIN

GWN 1004
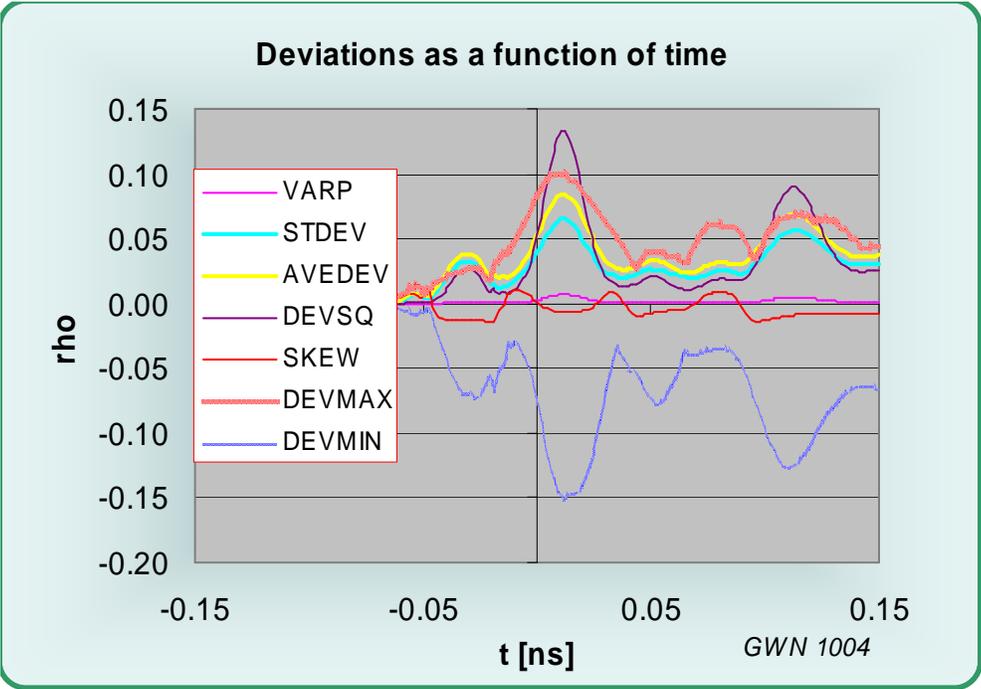
Figure 6 TDR signal from an OPEN: Statistics

More detail about the individual statistics can be found in the dc test report (cycling) and MSExcel. The maximum and minimum deviations from the average values are also shown (DEVMAX and DEVMIN = error bands).

Not surprisingly, values peak in the transition region.

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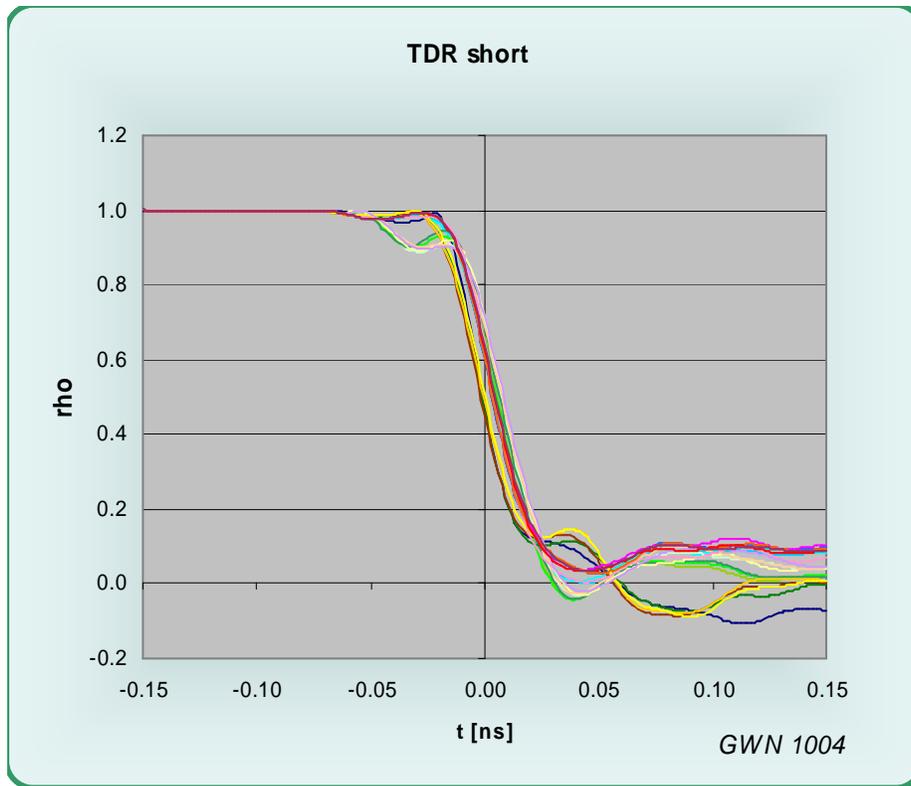
TDR short

Figure 7 TDR signal from a SHORT circuited CSP microstrip socket

   For the short circuited CSP microstrip socket the average fall time is 39.4 ps with a standard deviation of 12.6 ps. This is only a small increase over the system risetime of 49.5 ps. The average electrical length for this case is 3.6 ps with a standard deviation of 1.6 ps.

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Statistics for the short circuit response datasets yield the following results:
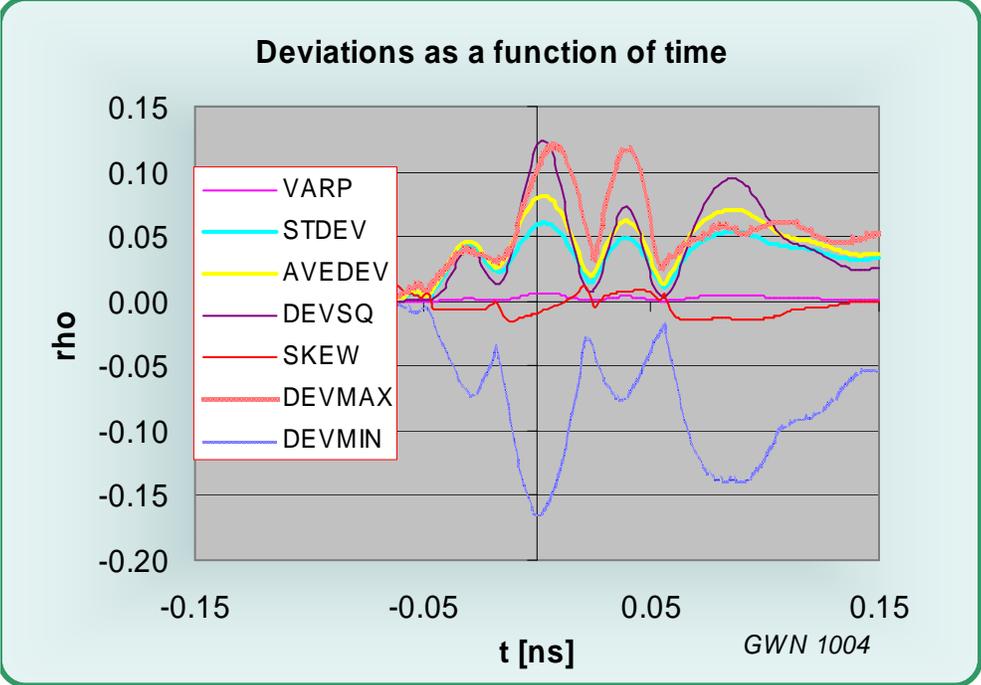
Figure 8 Short circuit dataset statistics

Deviations peak in the transition region, but show no abnormal values.

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TDR thru

GWN 1004
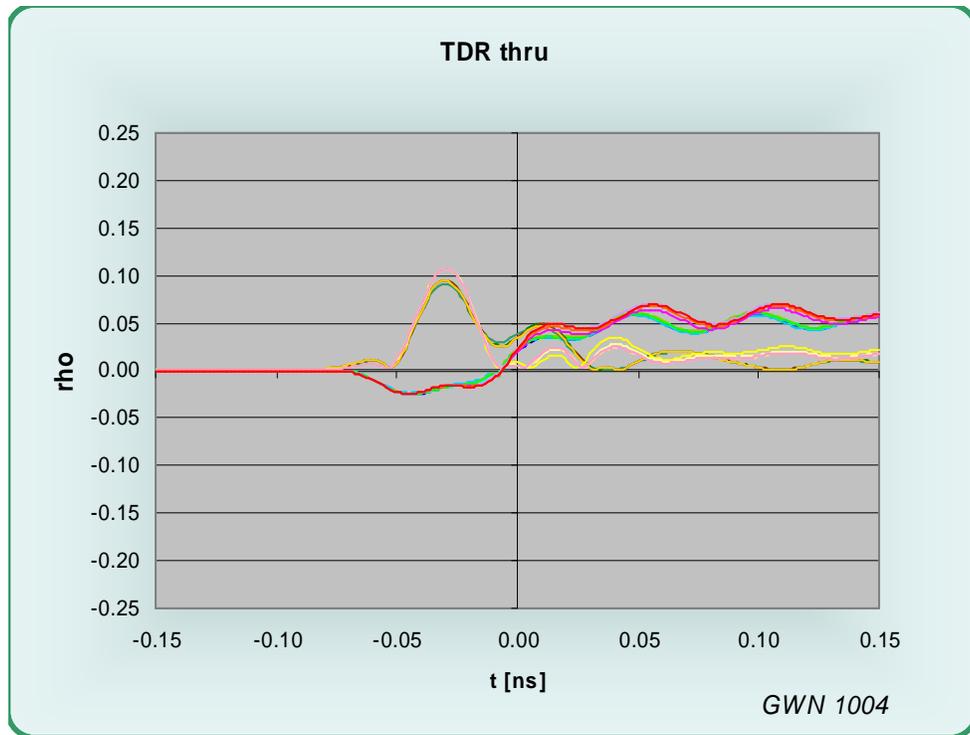
Figure 9 TDR measurement into a 50 Ohm probe

The thru TDR response shows both inductive and capacitive responses. The high peak average corresponds to a transmission line impedance of 58.6 Ohms, the low peak average (dip to negative values) to 48.6 Ohms. The standard deviations are 2.4 Ohms and 1.2 Ohms, respectively. The dip is possibly caused by fixture pad's presence to the socket material, which causes capacitive loading. When graphed, the following dependence of the peak on cycle number is obtained:

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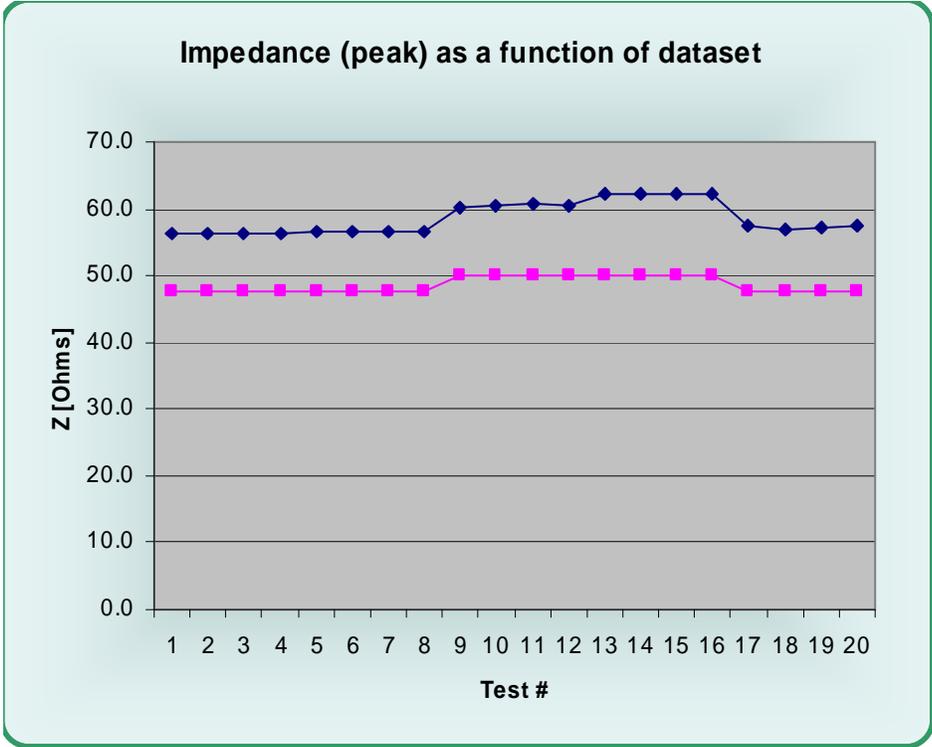
Figure 10 Thru impedance peaks as a function of test #

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The TDT performance for a step propagating through the pin arrangement was also recorded:

TDT

GWN 1004
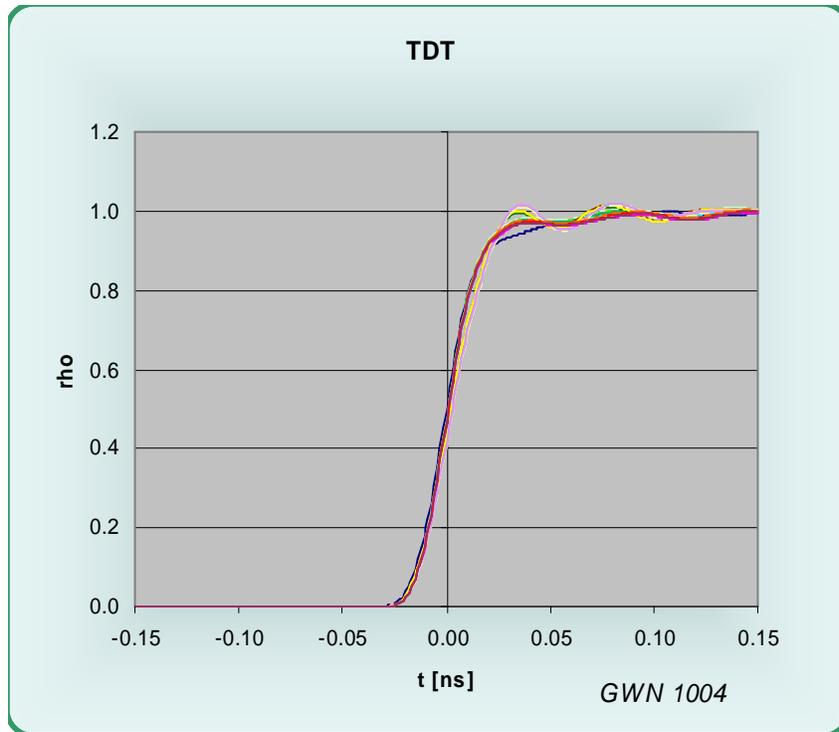
Figure 11 TDT measurement

The TDT measurements for transmission show a small contribution to risetime from the pin array (average 10-90% RT = 32.6 ps @ 1.4 ps STD DEV, the system risetime is 33.0 ps). The average added delay at the 50% point 1.5 ps with a standard deviation of 0.9 ps. There is no significant signal distortion.

A surface chart shows how the waveforms evolve as a function of the test number:

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TDT as a function of time and test #

GWN 1104
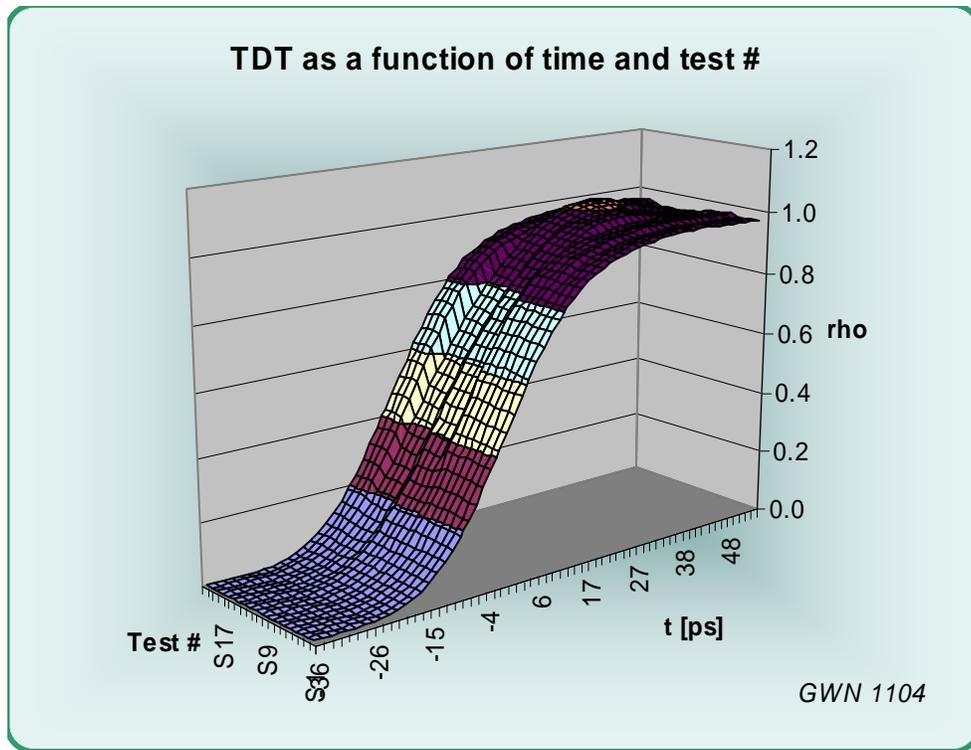
Figure 12 TDT measurement

The transmitted waveforms show little change with increasing cycle numbers.

The chart of the risetime as a function of cycle number shows no significant change with the number of test sequences:

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Thru risetime
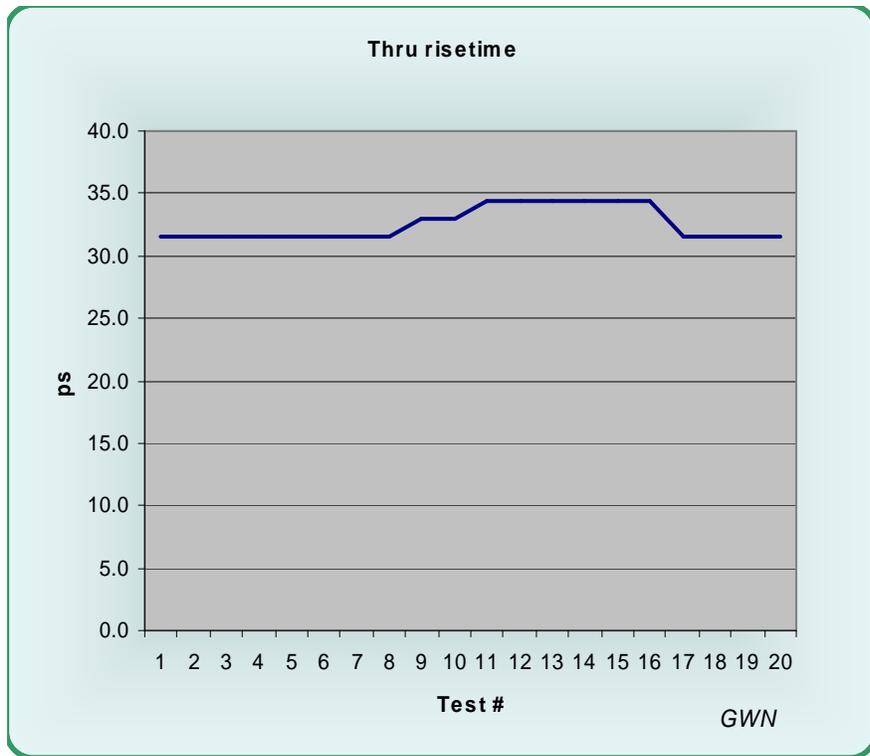
Figure 13 TDT risetime as a function of cycle number

No significant changes occur throughout the test. The slight rise for tests #9-16 is likely from a change in grounding of adjacent microstrip lines.

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Frequency domain

Network analyzer reflection measurements for a single sided drive of the signal pin with all other pins open circuited at the opposite end were performed to determine the pin capacitance. The analyzer was calibrated to the end of the probe and the phase of S11 was measured. From this curve the capacitance of the signal contact to ground can be determined (see below).
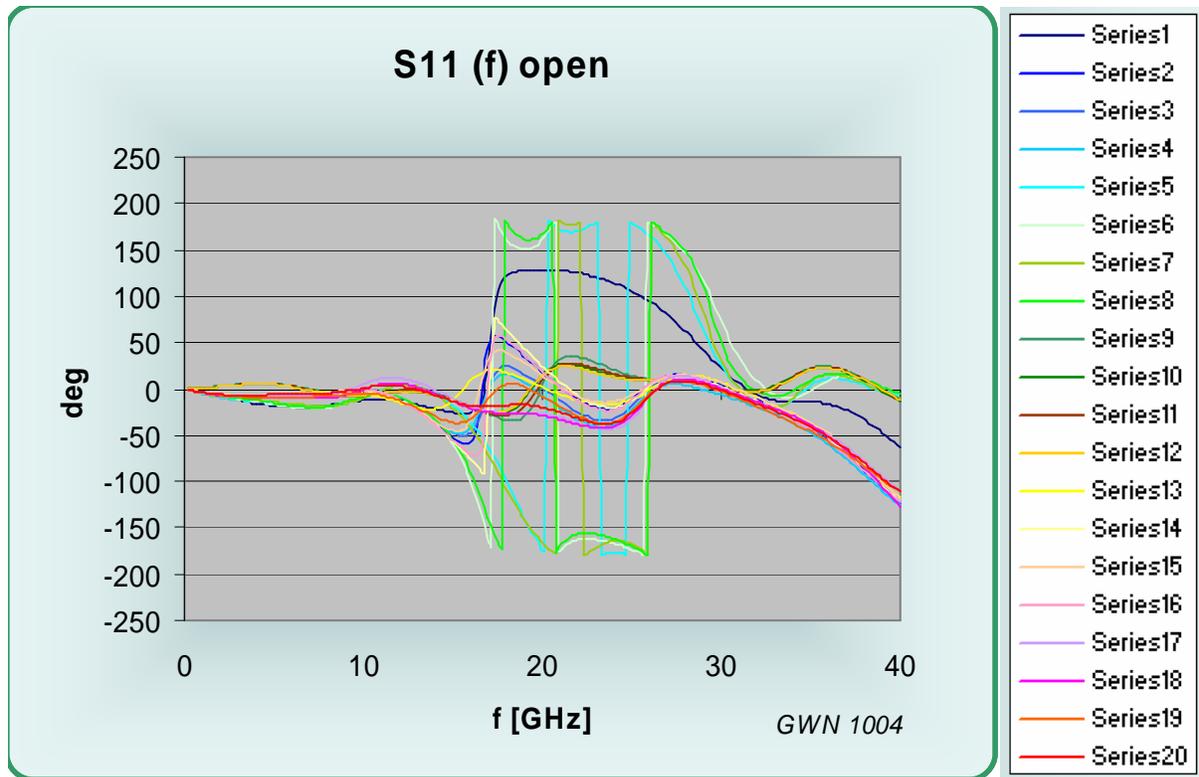
Figure 14 S11 phase (f) for the open circuited signal pin

A number of cycles show phase jumps. These occur in the vicinity of a resonance caused by a parasitic transmission line (see test methodology).

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S11(f) open

GWN 1004
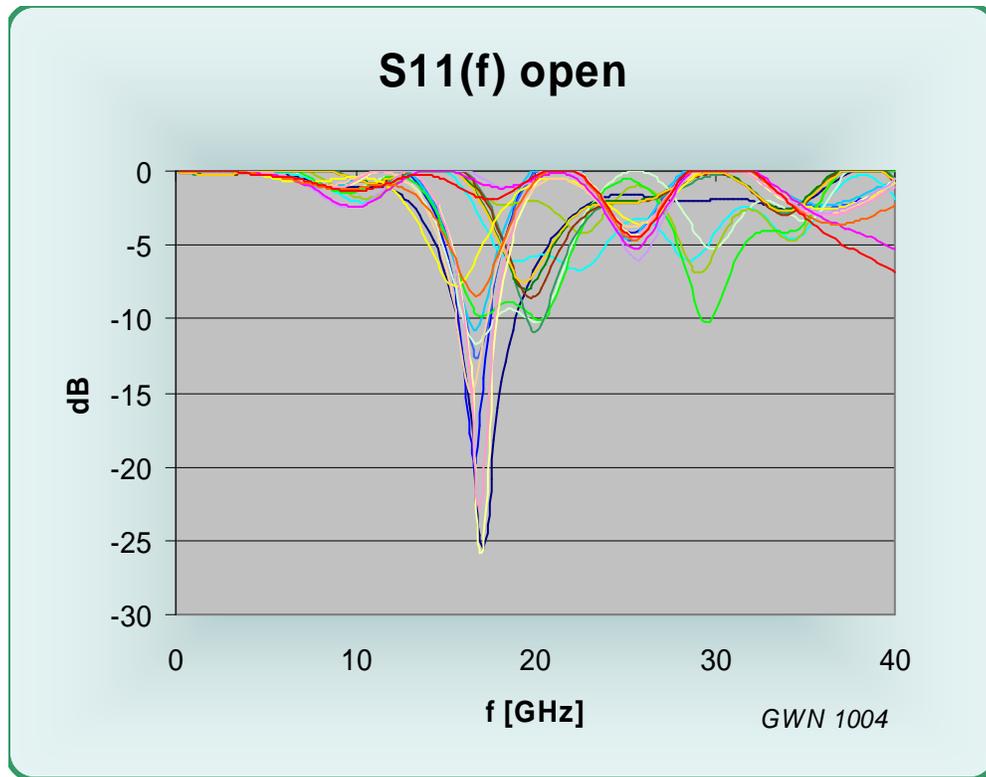
Figure 15 S11 magnitude (f) for the open circuited signal pin

While ideally the magnitude of S11 should be unity (0 dB), loss, radiation and resonances in the array are likely contributors to noticeable return loss for the open circuited pins at elevated frequencies. As in case of the phase above, a connection uncertainty causes a parasitic transmission line. It is possibly specific to the test setup used here.

A 3D representation of the open circuit return loss shows how this loss evolves with increasing sequence number (S1-S20). The chart is inverted since S11 cannot be greater than 0 dB:

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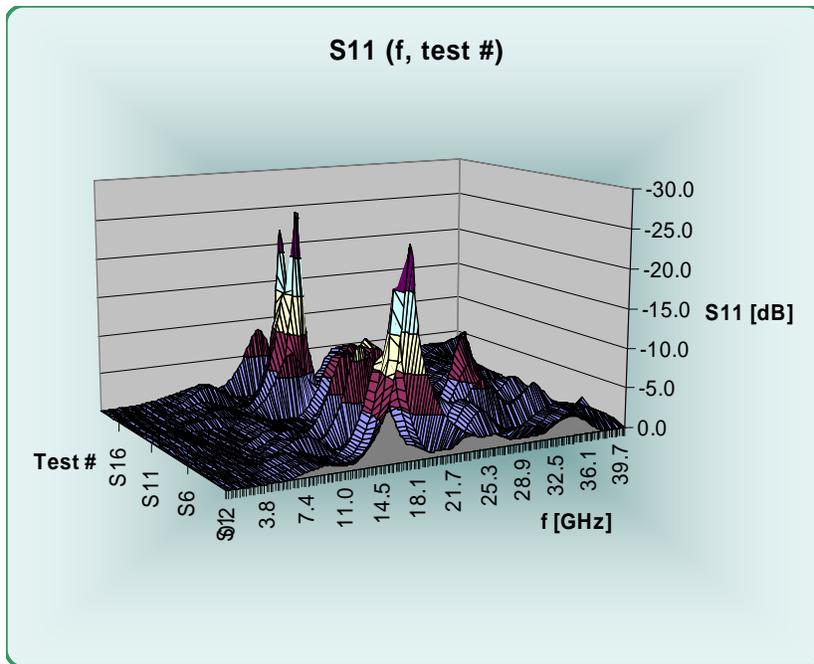
Figure 16 S11 magnitude (f) for the open circuited signal pin

Resonance conditions like the one observed at 18 GHz are particularly sensitive to small changes in the setup, the socket and the instrument calibration. Thus deviations recorded in the datasets for each frequency (cycle1 thru 20) displayed as a function of frequency (definitions can be found in MSExcel and the dc test report) also increase:
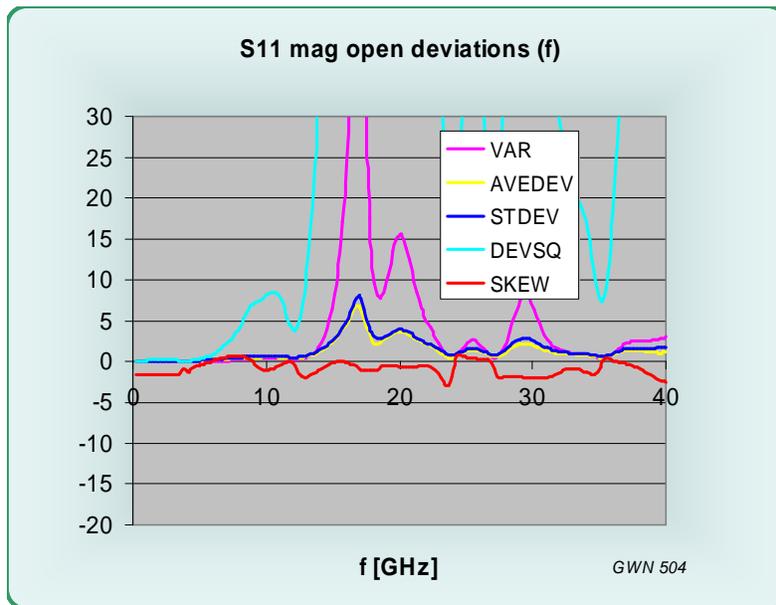
Figure 17 S11 magnitude deviations (f) for the open circuited signal pin

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When calculating the capacitance of the signal pin with respect to ground from the measurements, the following results are obtained:

C(f)
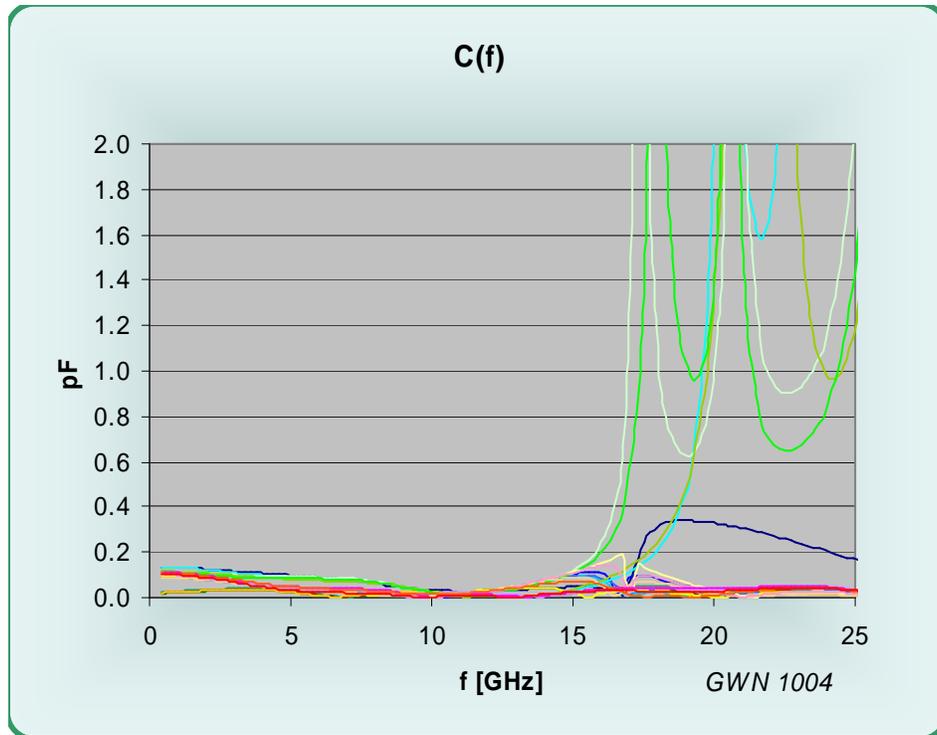
Figure 18 C(f) for the open circuited signal pin

The average capacitance is 0.09 pF at low frequencies. Standard deviation is 0.033 pF. Scatter is due to the undetermined ground reference mentioned earlier. Above 15 GHz the parasitic line resonances invalidate the evaluation for some datasets.

The Smith chart measurement for the open circuit shows these parasitic line resonances:

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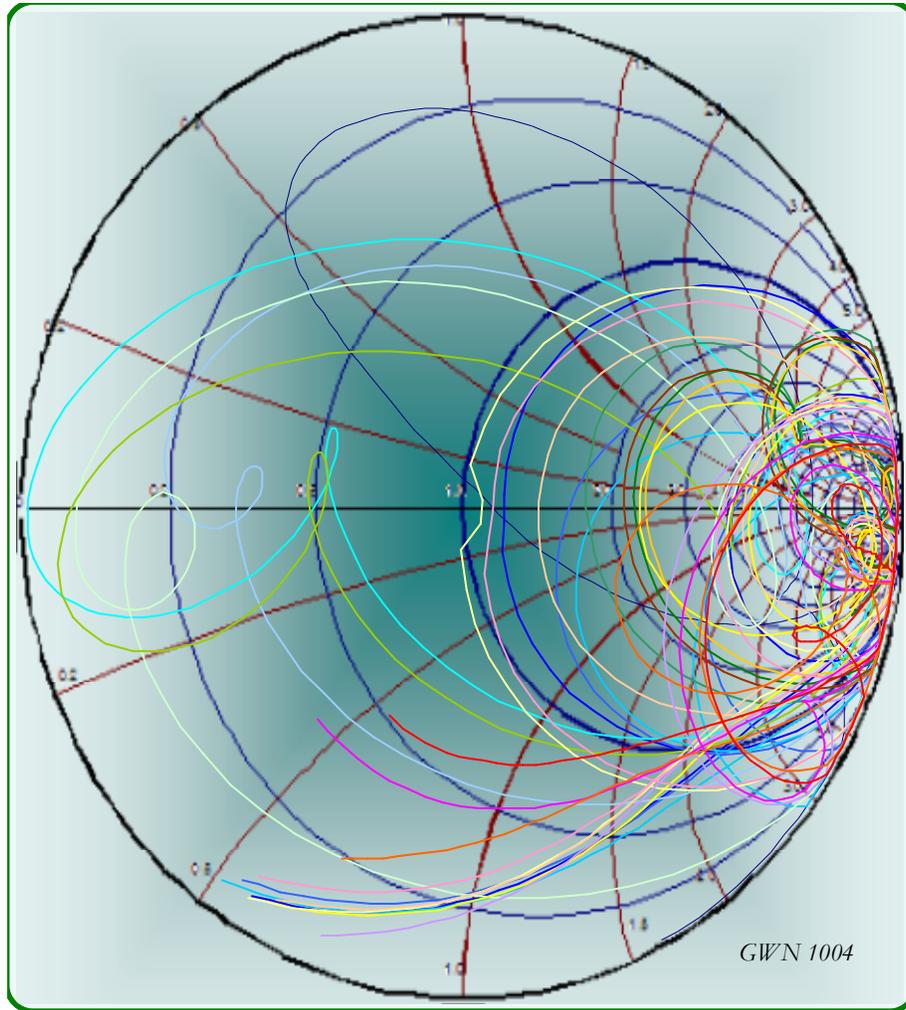
Figure 19 Reflections from the open circuited CSP microstrip socket

   To extract the pin inductance, the same types of measurements were performed with a shorted pin array. Shown below is the change in reflections from the CSP microstrip socket. Variability is again attributed to parasitic transmission lines (see above). Phase jumps of 360 degrees are due to the VNA.

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Figure 20 S11 phase (f) for the short circuited case
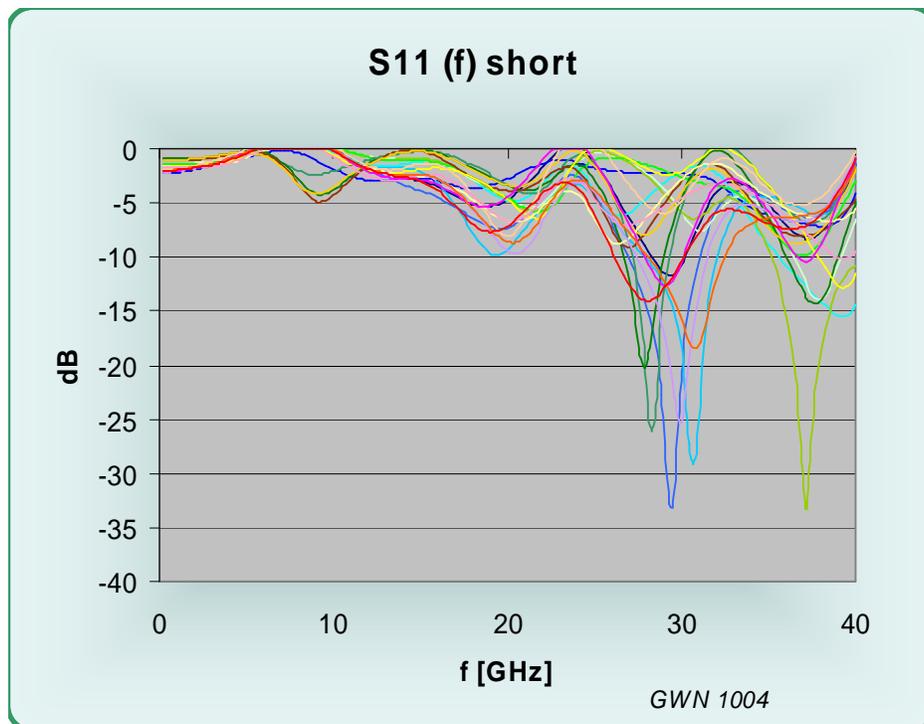
Figure 21 S11 magnitude (f) for the short circuited case

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A 3D plot reveals trends with increasing test numbers:

S11 (f, test #)
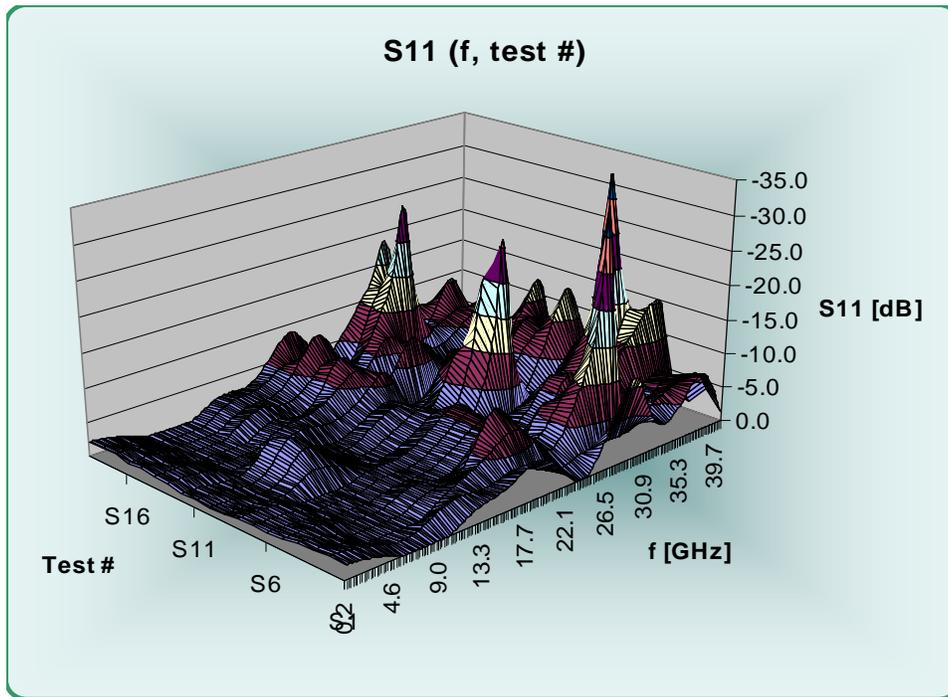
Figure 22 S11 magnitude (f) for the short circuited case

S11 mag short deviations (f)

- VAR
- AVEDEV
- STDEV
- DEVSQ
- SKEW

f [GHz]

GWN 504
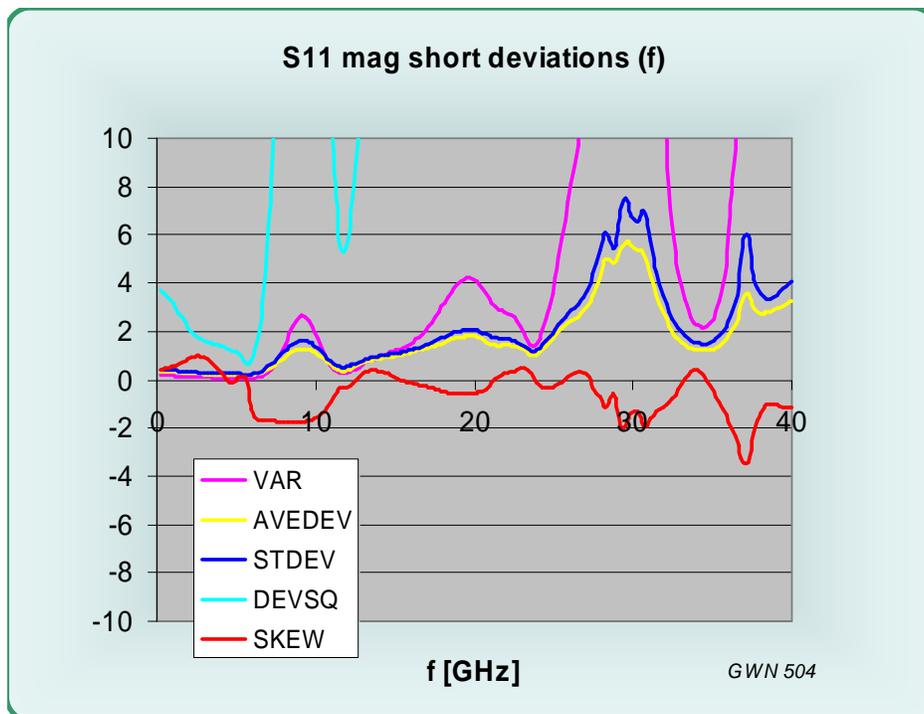
Figure 23 S11 magnitude deviations (f) for the short circuited case

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From these measurements the inductance of the pin can be extracted. Its evolution with frequency is shown below:

L(f)
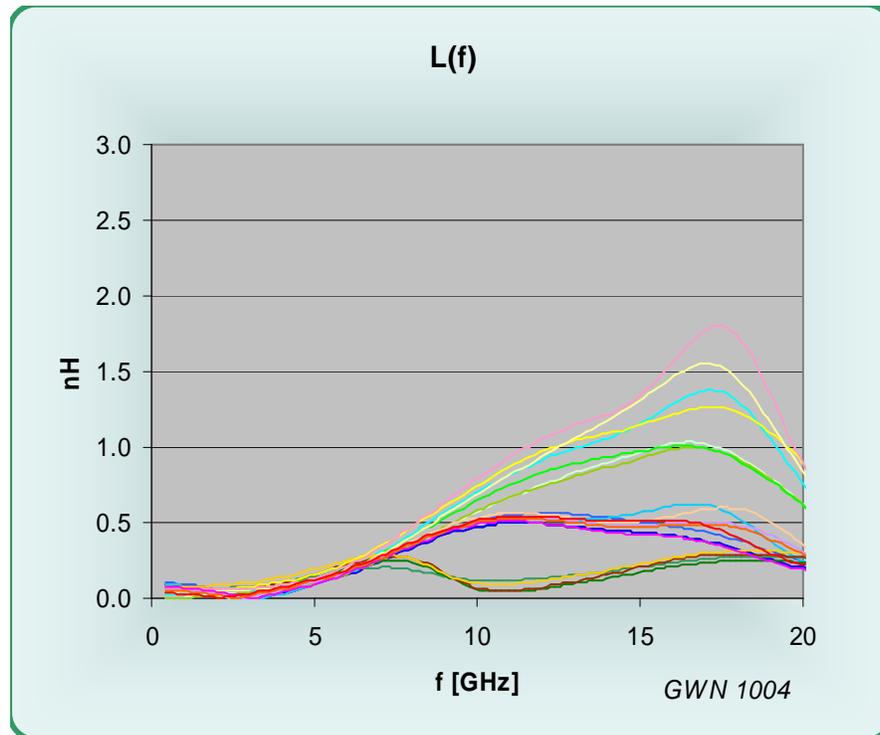
Figure 24 L(f) for the CSP microstrip socket

The phase changes recorded correspond to an average inductance of 0.05 nH at low frequencies. A standard deviation of 0.02 pH exists. The inductance rise toward 6 GHz is likely again due to the fact that parasitic transmission lines are coupling to the microstrip.

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This is also witnessed by the display of S11 in the Smith chart:
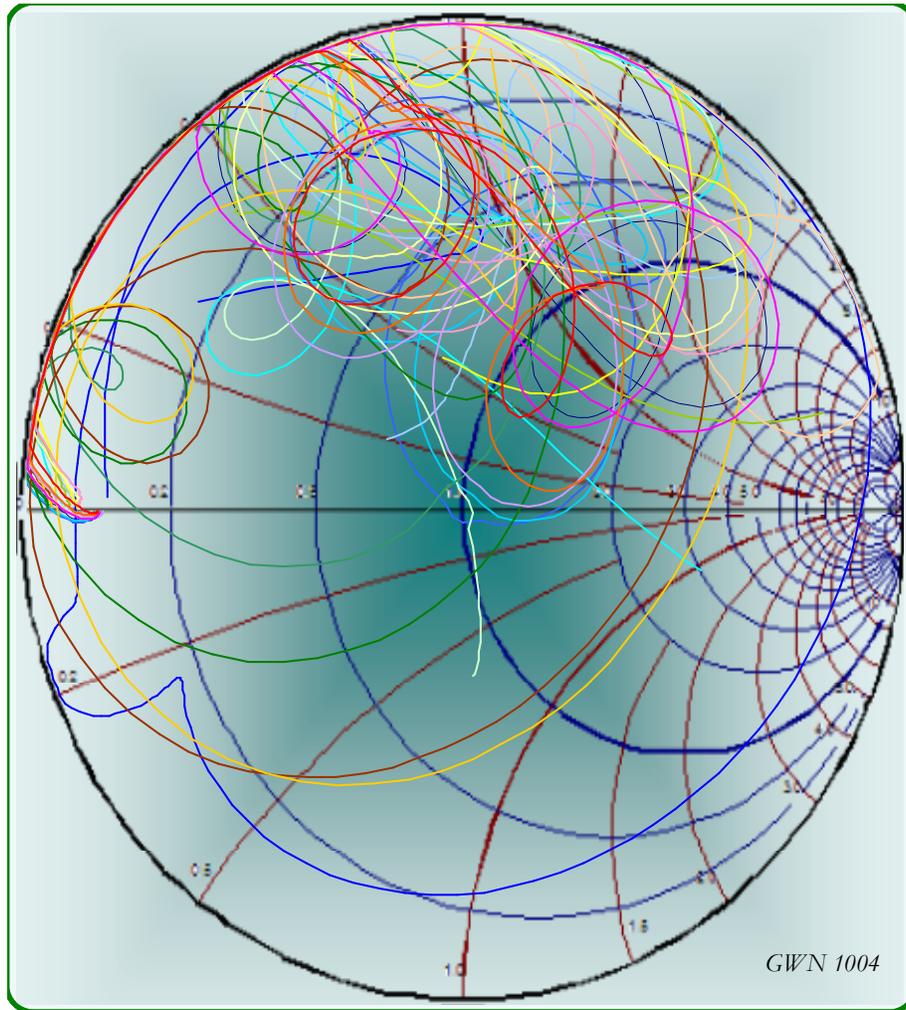
Figure 25 Short circuit response in the Smith chart

Resonances are noticeable in the Smith chart for the short circuit condition for those traces that are afflicted by parasitic transmission lines.

An insertion loss measurement is shown below for the frequency range of 50 MHz to 40 GHz.

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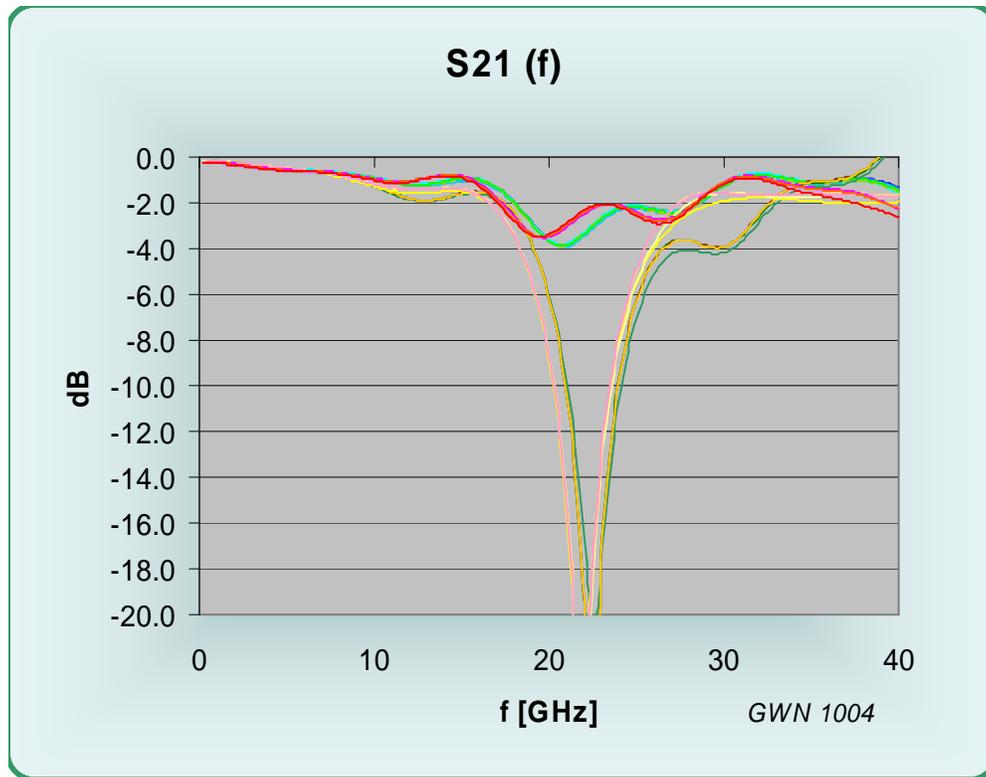
Figure 26 Insertion loss S21 (f)

Insertion, like other parameters before, shows some variation.

A 3D plot shows how S21 evolves with cycling:

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S21 (f, test #)
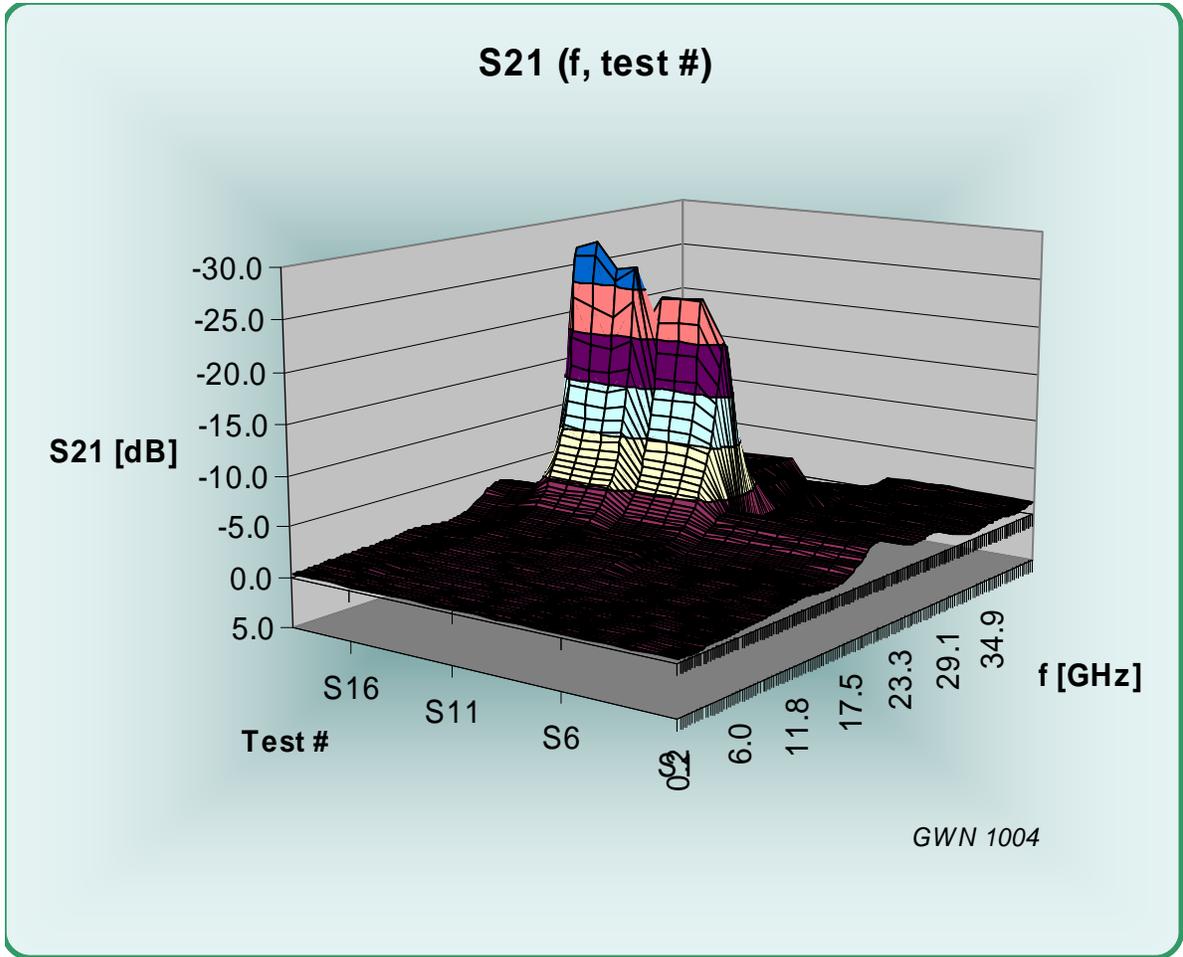
Figure 27 Insertion loss S21 (f) as a function of cycle #

Deviations in the datasets for each frequency point from cycle 1 to 20 are recorded as a function of frequency and also reveal this as follows:
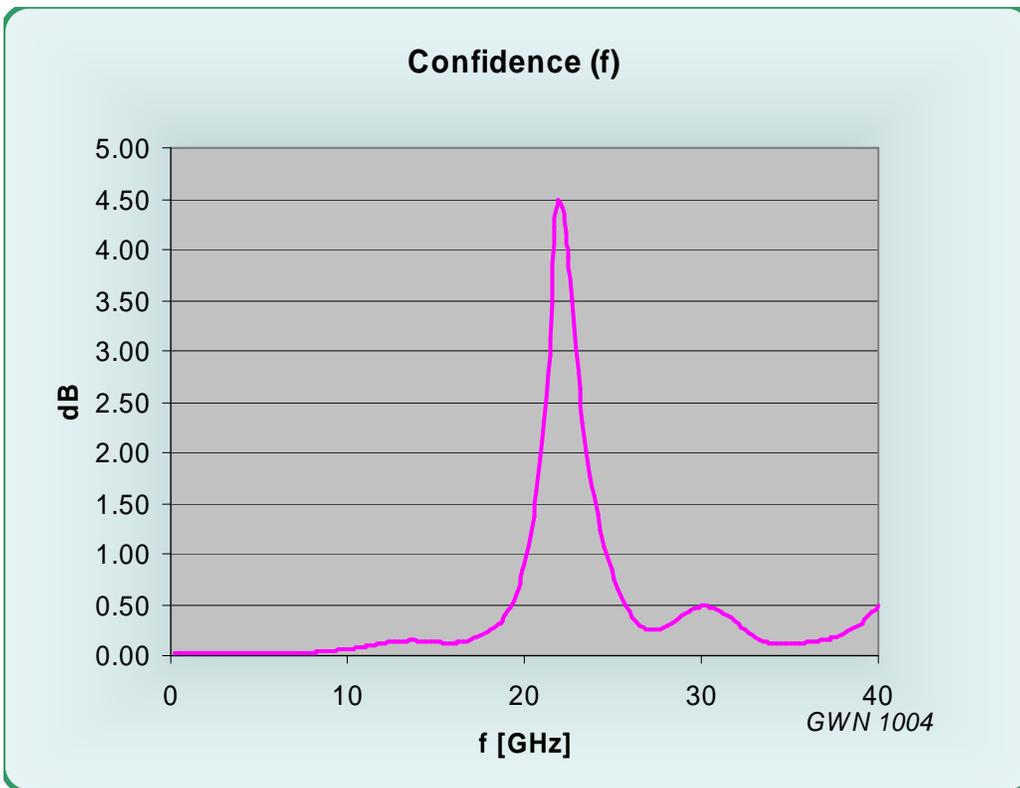
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S21 deviations (f)

Legend: VAR, AVEDEV, STDEV, DEVSQ, SKEW

f [GHz]

GWN 1004
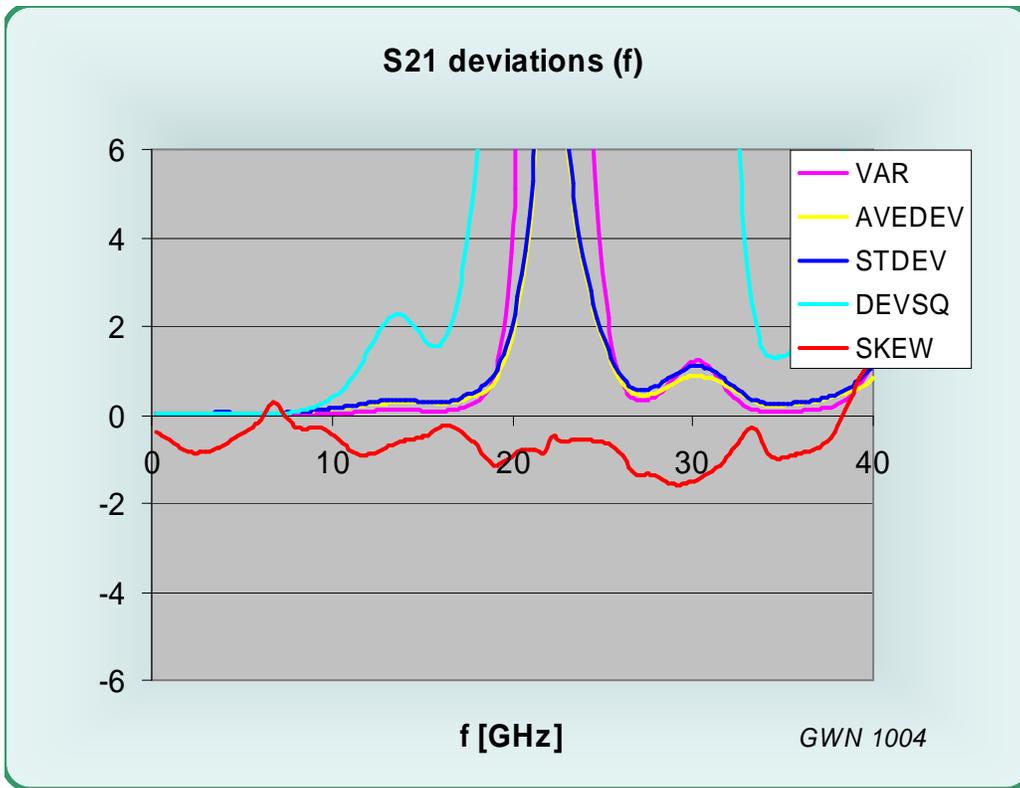
Figure 28 and 29   Insertion loss S21 (f) deviations

Confidence (f)

dB

f [GHz]

GWN 1004

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The confidence interval in the S21 figure above indicates the range on either side of the sample mean for which one can be 95% sure that test results will fall within that range.
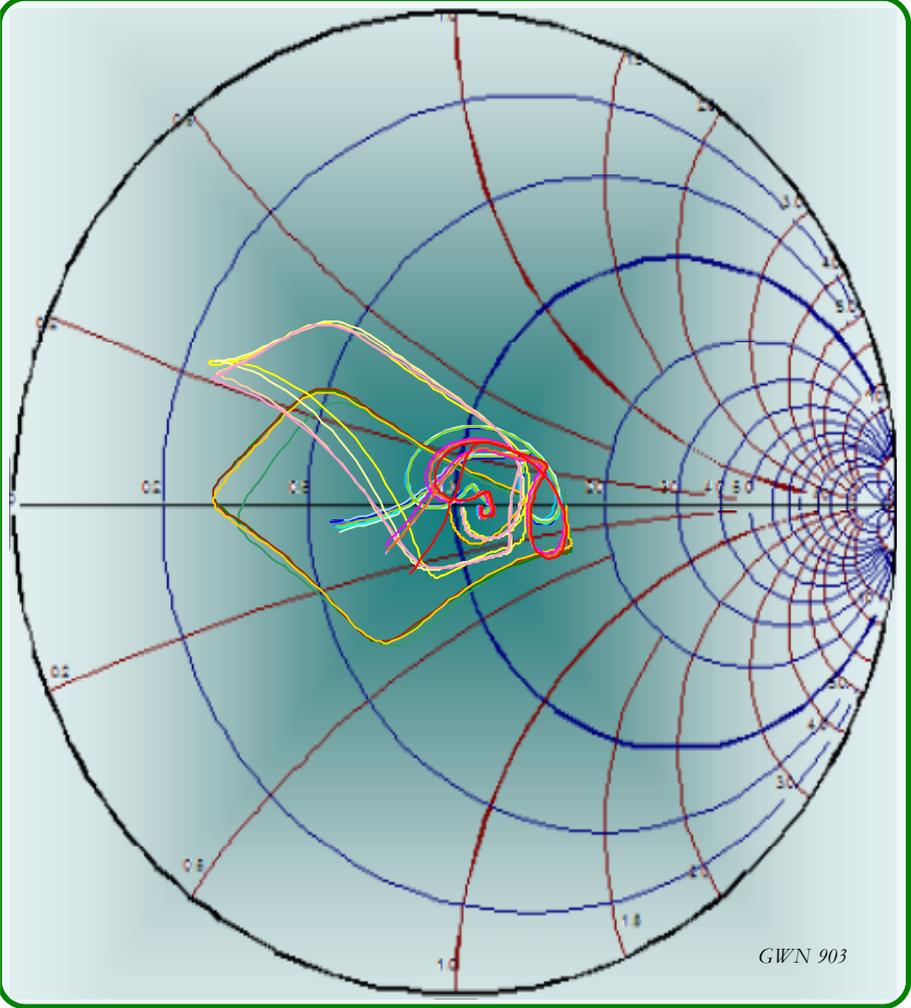
Figure 30 Smith chart for the thru measurement into a 50 Ohm probe

The Smith chart for the thru measurements shows a reasonable match with some reactive components except for those tests where resonances are present.

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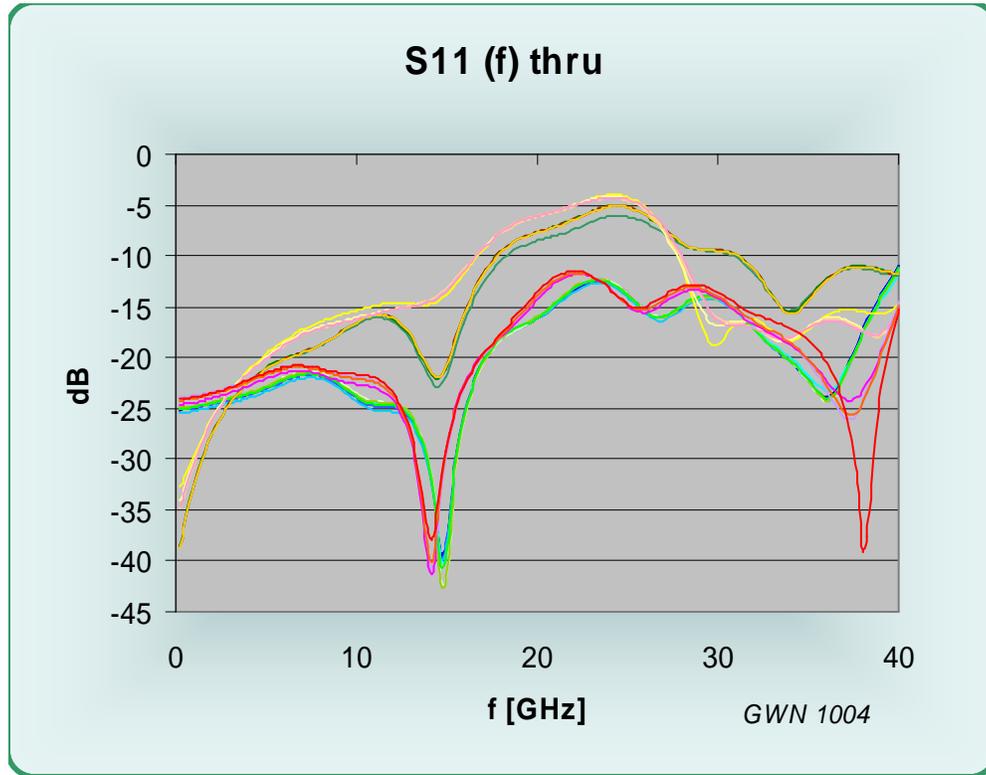
Figure 31 S11 magnitude (f) for the thru measurement into a 50 Ohm probe

Some changes occur throughout the cycling program. This is also visible in a 3D plot and the statistics as seen in the graphs below. In particular, the squares of deviations show strong variations at low frequencies. This is not very meaningful, however, since even the slightest change in conditions will immediately affect the return loss at these very low signal values. In practical operation, as long as the overall S11 value is low, such changes will have no significance.

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S11 (f, test #)
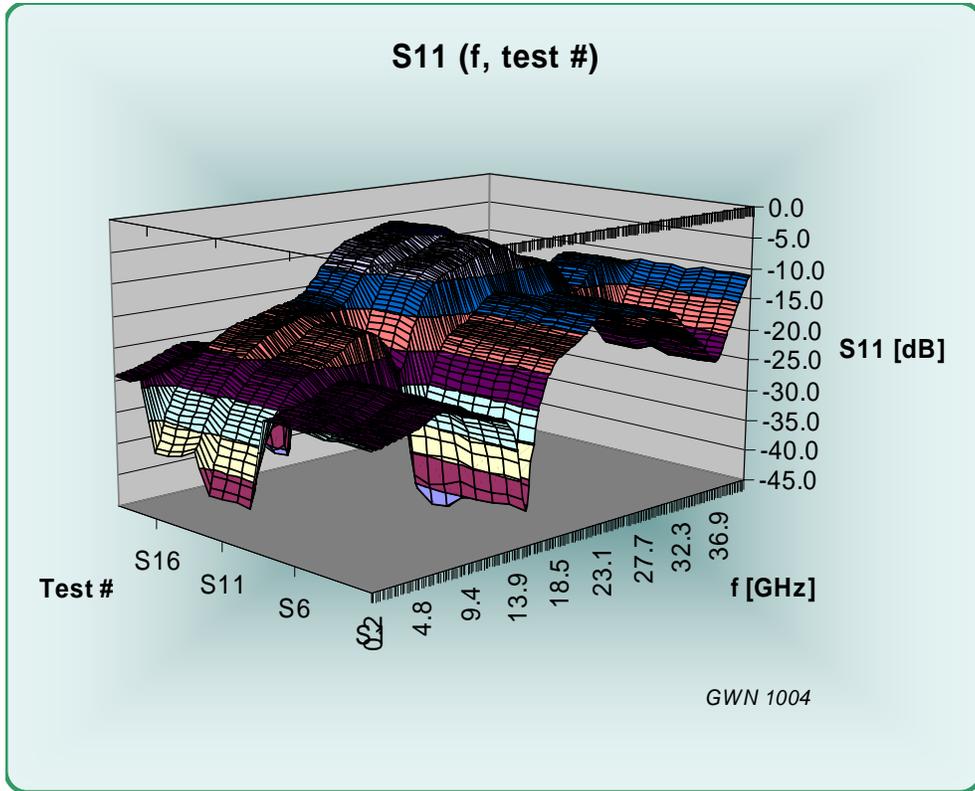
Figure 32 S11 magnitude (f) for the thru measurement into a 50 Ohm probe

S11 mag thru deviations (f)
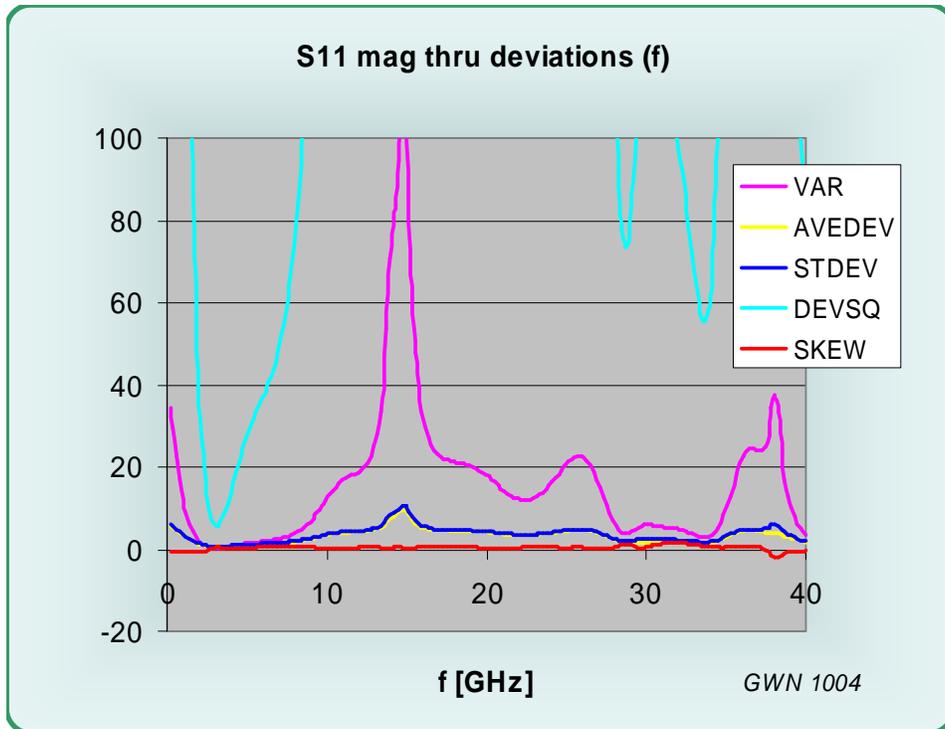
Figure 33 S11 magnitude (f) for the thru measurement into a 50 Ohm probe

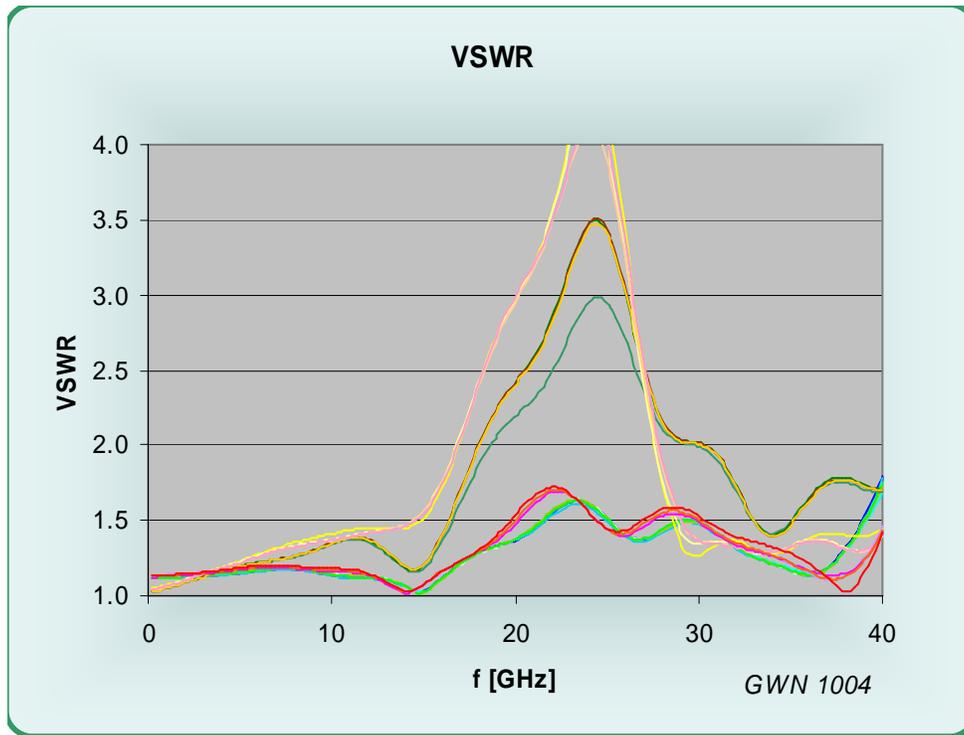*GateWave Northern, Inc.*

VSWR

Figure 34 Standing wave ratio VSWR (f) [1 / div.]

On average, the VSWR remains below 1.2 : 1 to a frequency of 11.9 GHz and is less than 2 : 1 for frequencies below 31.0 GHz. The standard deviations for these numbers throughout the cycling are 6.0 and 11.4, respectively.

Crosstalk was measured in the G-S-S-G configuration by feeding the signal pin and monitoring the response on an adjacent pin. Measurement results can be found in the section on the G-S-S-G configuration.

Measurements G-S-S-G

Time domain

Again, the time domain measurements will be presented first. A TDR reflection measurement is shown here for the thru case at port 1 to port 2:
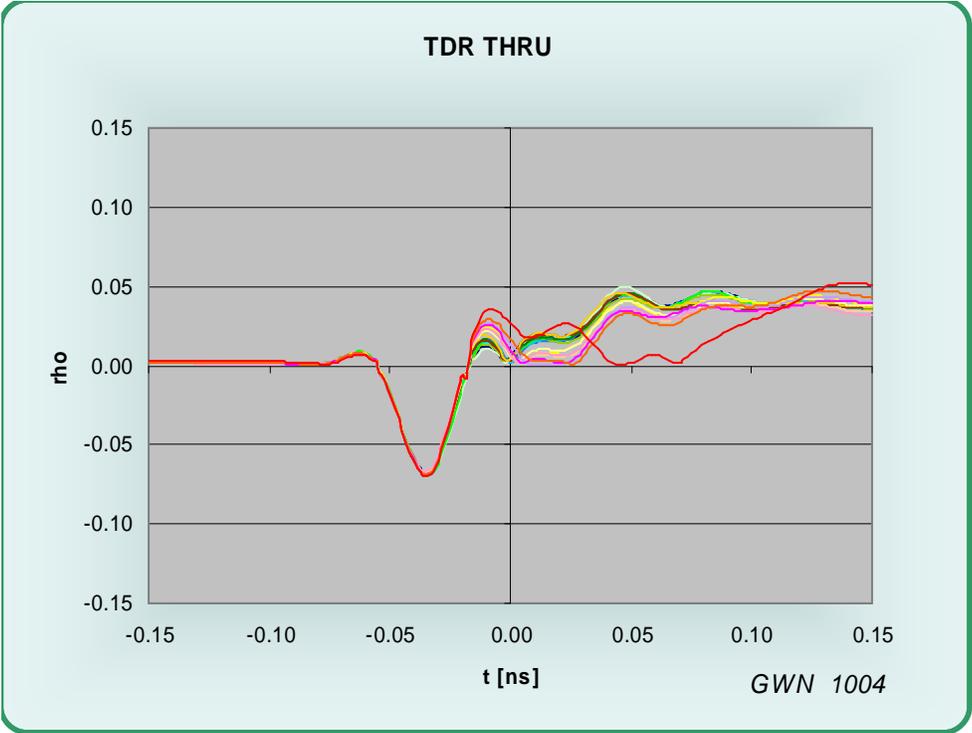

TDR THRU

GWN 1004

Figure 35 TDR through socket into a terminated probe

The thru TDR response shows both inductive and capacitive responses.   The average peak corresponds to a transmission line impedance of 54.8 Ohms at a standard deviation of 0.4 Ohm. The average low point is 43.6 Ohms with a STDEV of 0.1 Ohm. The peak is higher than in the GSG case, most likely because of the fact that one of the adjacent pins is not grounded. Relatively little change occurs with cycle number.

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The TDT performance for a step propagating through the G-S-S-G pin arrangement was also recorded:
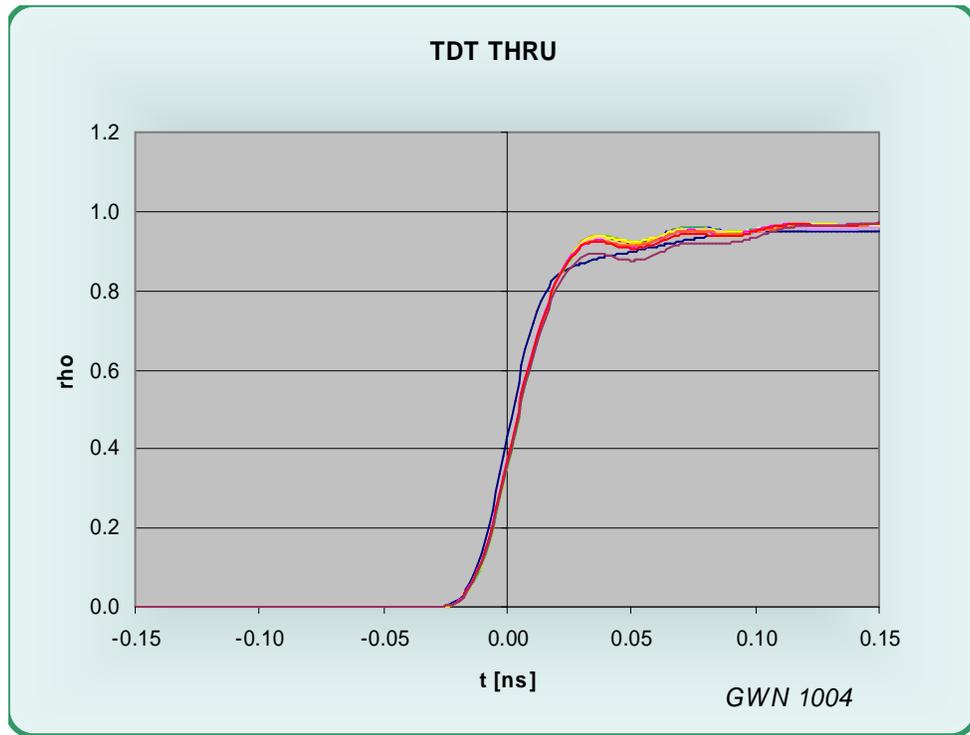

TDT THRU

GWN 1004

Figure 36 TDT measurement

The TDT measurements for transmission show some contribution to risetime from the pin array (average 10-90% RT = 35.0 ps, 1.1 ps STDEV, the system risetime is 37.5 ps). The likely source for a greater system risetime is the elevated impedance of the microstrip without the socket present. The average added delay at the 50% point is 3.0 ps at 0.5 ps standard deviation.

Shown below is a surface representation of this graph as test numbers increase:

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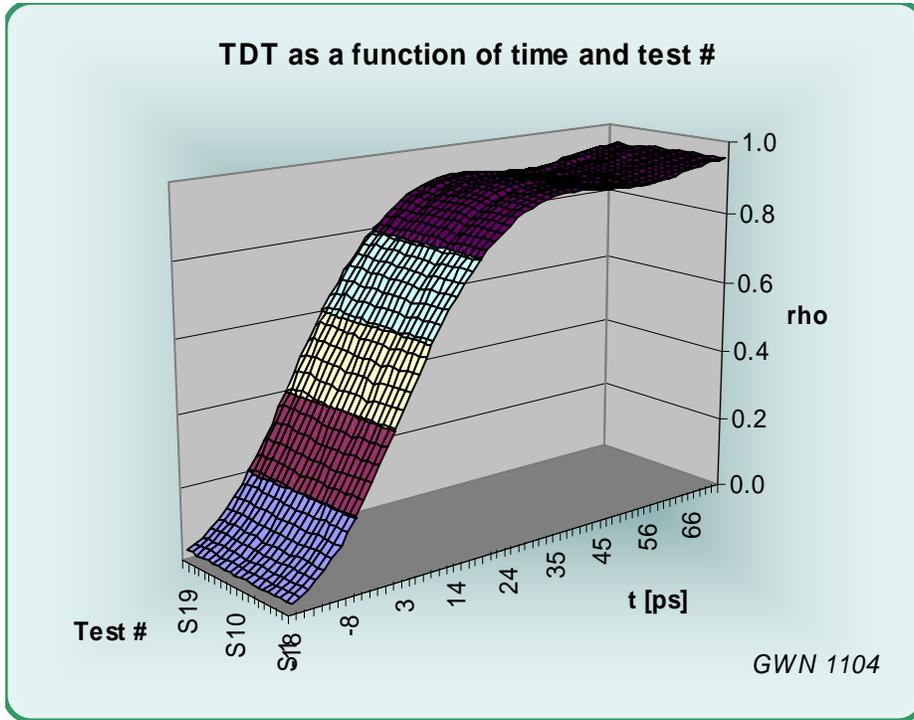
Figure 37 TDT measurement GSSG

There are no significant changes throughout the test program.   Also shown below are the deviations as a function of time:
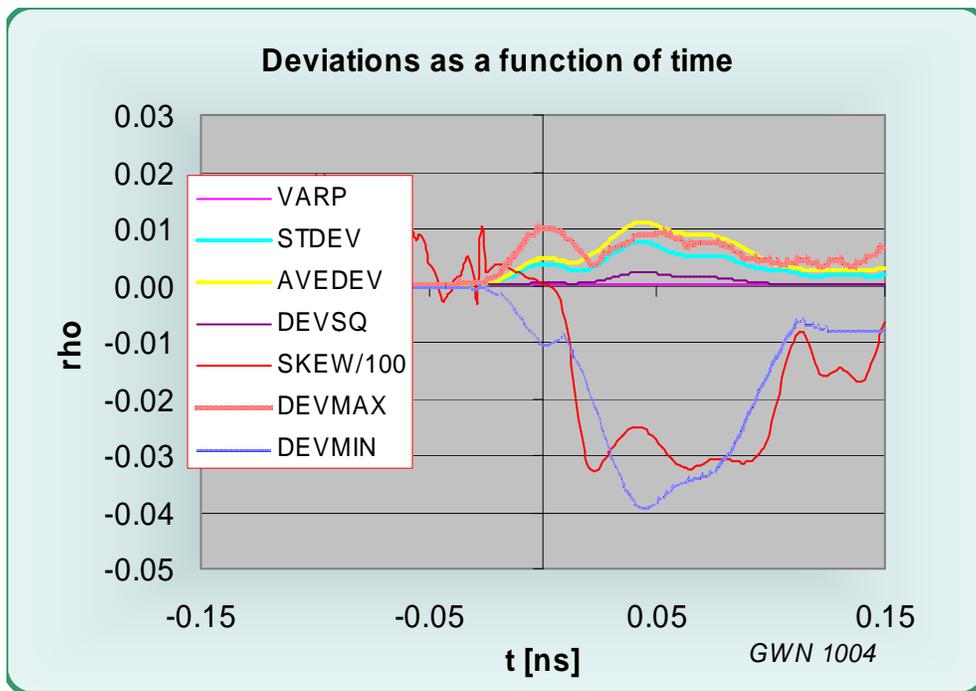

Figure 38 TDT measurement GSSG deviations from mean

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Frequency domain

Network analyzer reflection measurements for the G-S-S-G case were taken with all except the pins under consideration terminated into 50 Ohms. As a result, the scattering parameters shown below were recorded for reflection and transmission through the contact array.

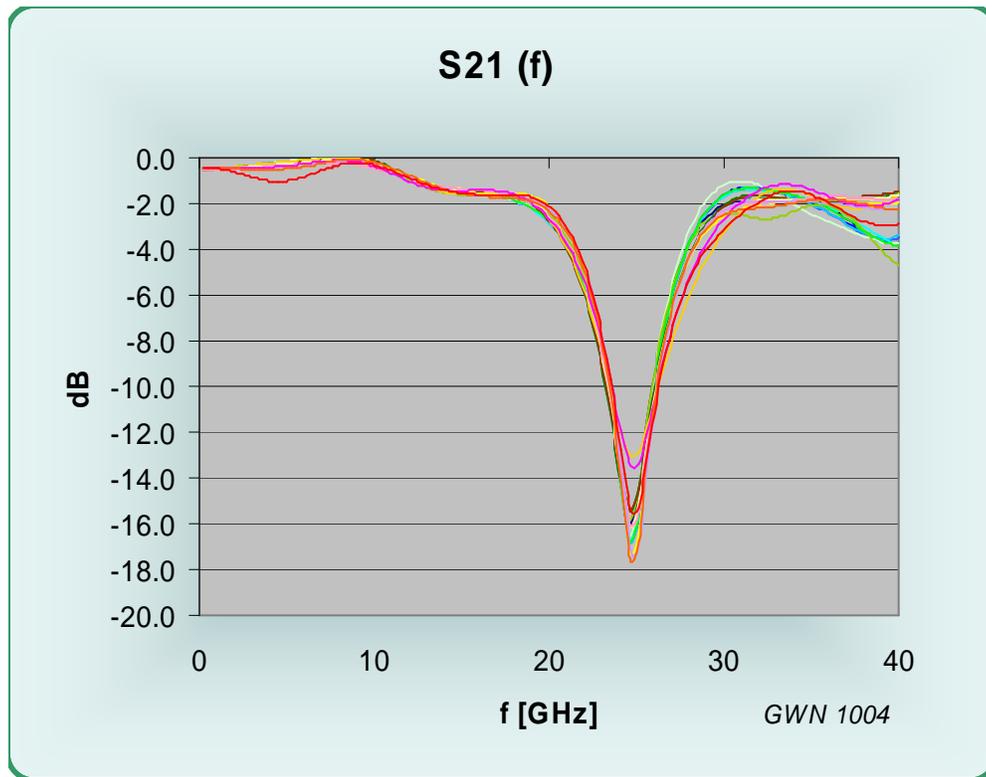First, insertion loss measurements (S21 and S12) are shown for port 1 to port 2.

Figure 39 Insertion loss S21 (f) GSSG

Insertion loss evolution toward higher cycle numbers shows no significant changes. Here, a resonance thought to be caused by a parasitic transmission line was present through all tests. A surface representation (with inverted axes) is shown below:
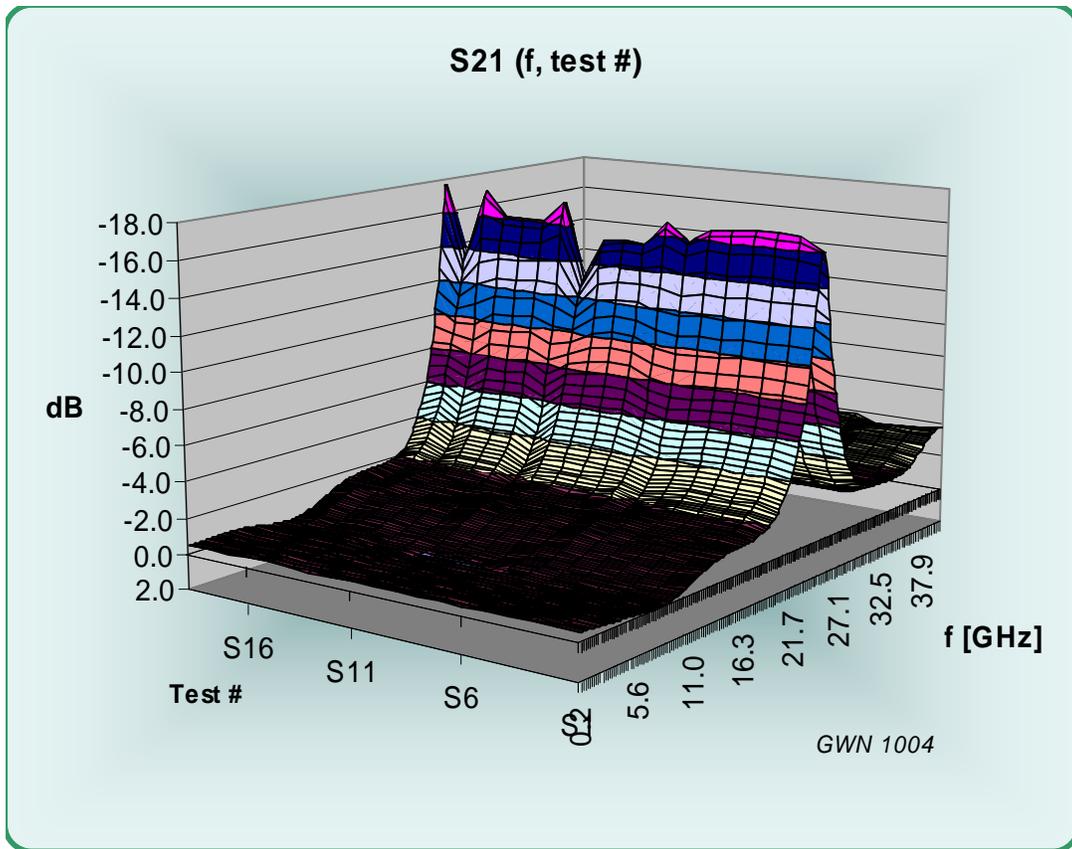
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Figure 40 Insertion loss S21 (f) GSSG

The deviations from mean in the datasets as a function of frequency is as follows:

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S21 deviations (f)
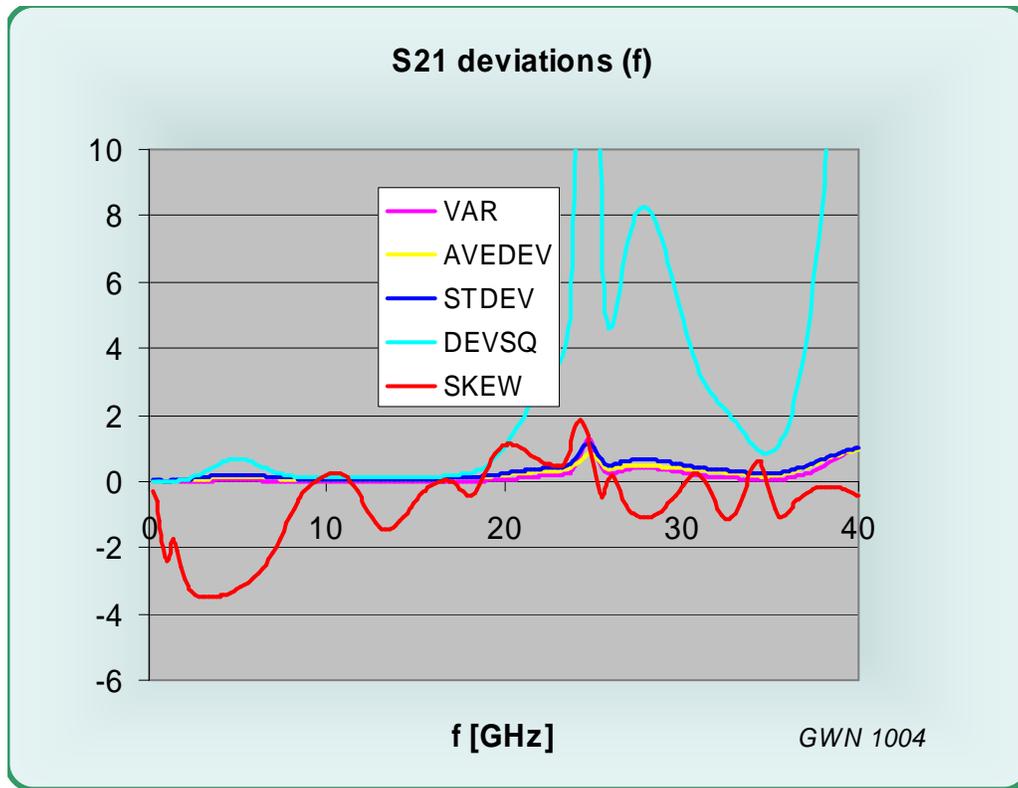
Legend: VAR, AVEDEV, STDEV, DEVSQ, SKEW

GWN 1004

Figure 41 Insertion loss S21 (f) deviations

The squares of deviations value rises at 25 GHz, likely signifying increased sensitivity because of the resonance.
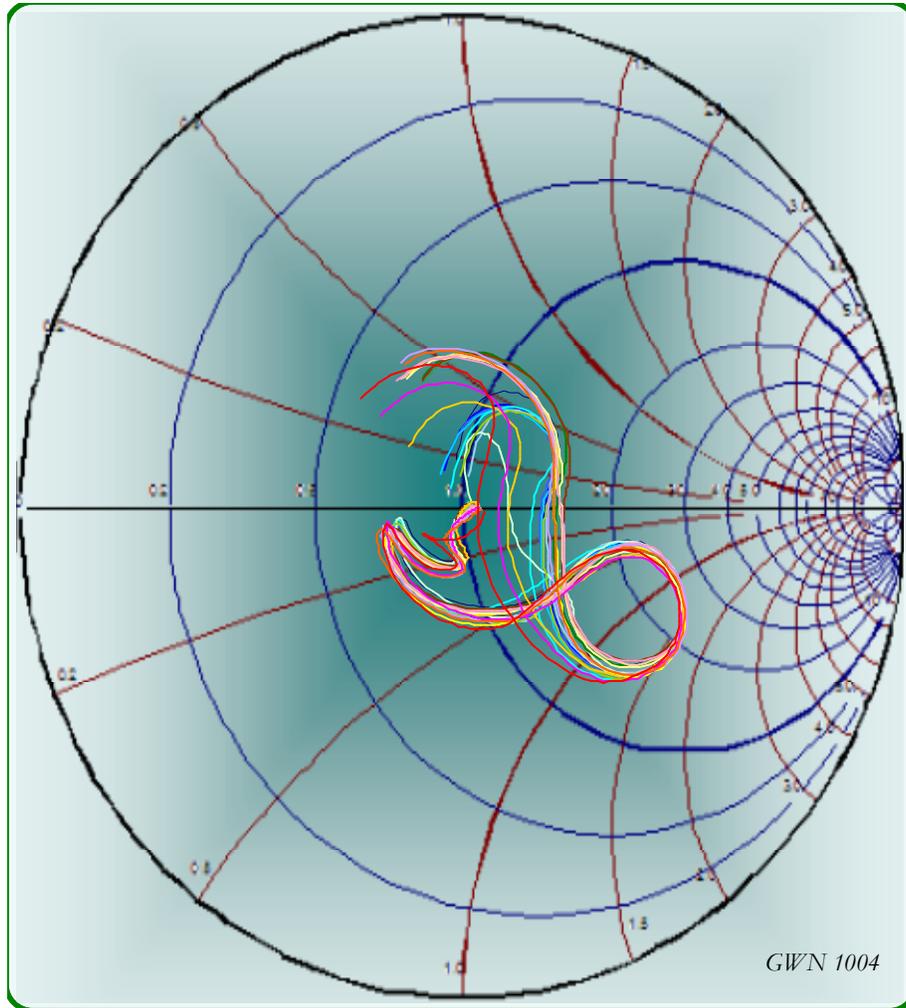
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Figure 42 Smith chart for the thru measurement into a 50 Ohm probe

The Smith chart for the thru measurements shows reactive components toward 40 GHz.
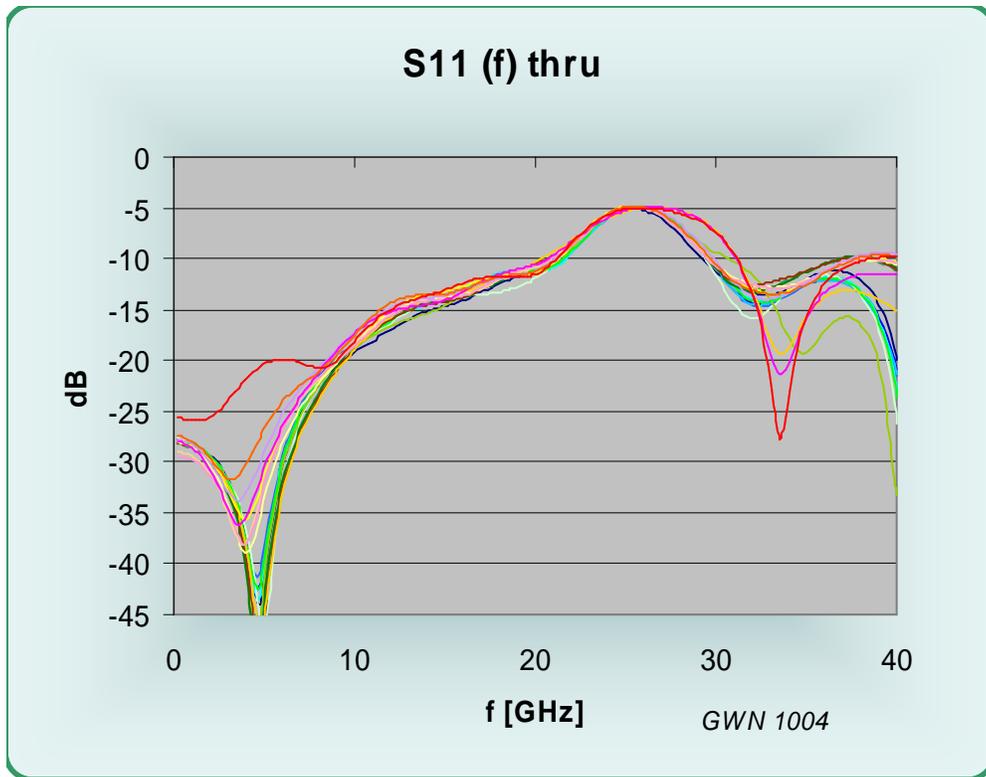
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Figure 43 S11 magnitude (f) for the thru measurements into a 50 Ohm probe

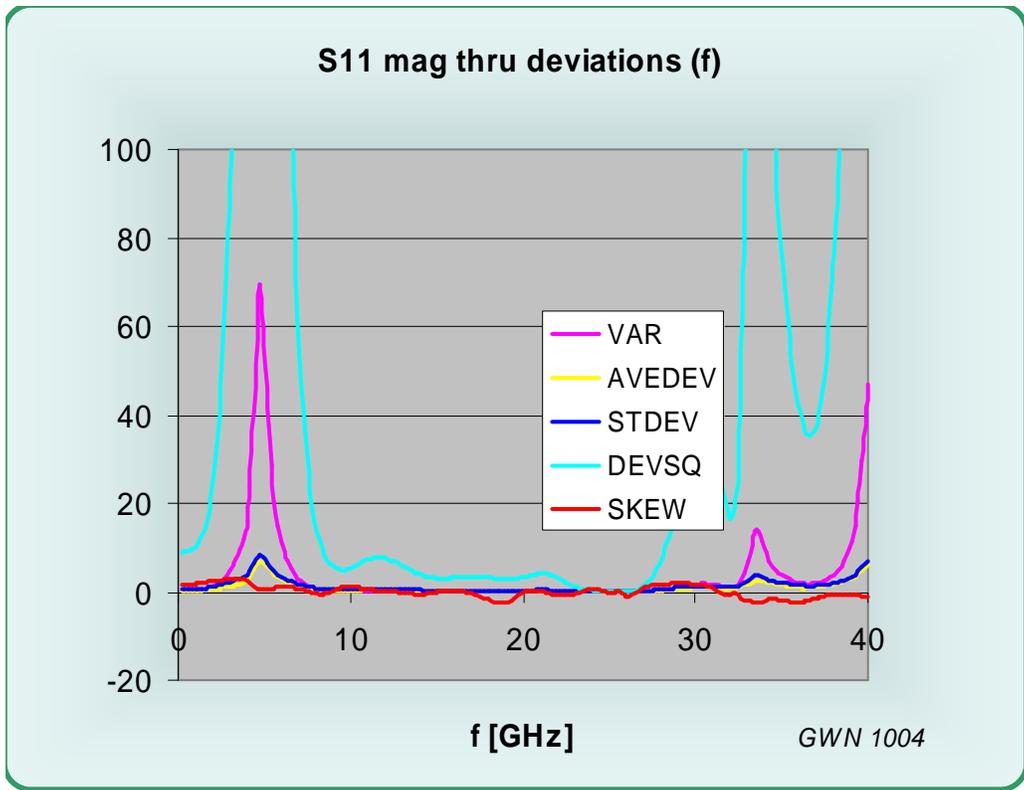Only for the highest cycle numbers does the return loss show some small changes.

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S11 mag thru deviations (f)

Figure 44 S11 magnitude (f) deviations (thru measurements into 50 Ohms)
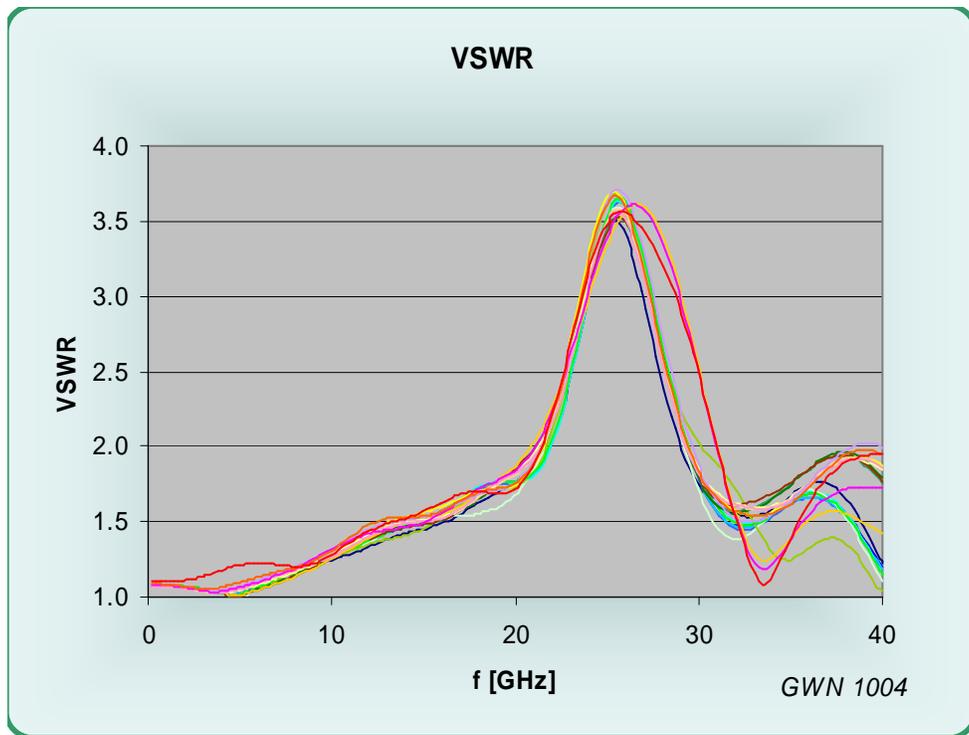
VSWR

Figure 45 Standing wave ratio VSWR (f) [1 / div.]

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The VSWR remains on average below 1.2 : 1 to a frequency of 8.3 GHz (STDEV = 0.9 GHz) for S11 and on average below 2 : 1 up to 36.2 GHz (7.7 GHz STDEV; end of sweep range).

When recording the crosstalk, two cases must be considered: Forward crosstalk (S41 in the notation used here) and backward crosstalk (S31 in the notation used here):
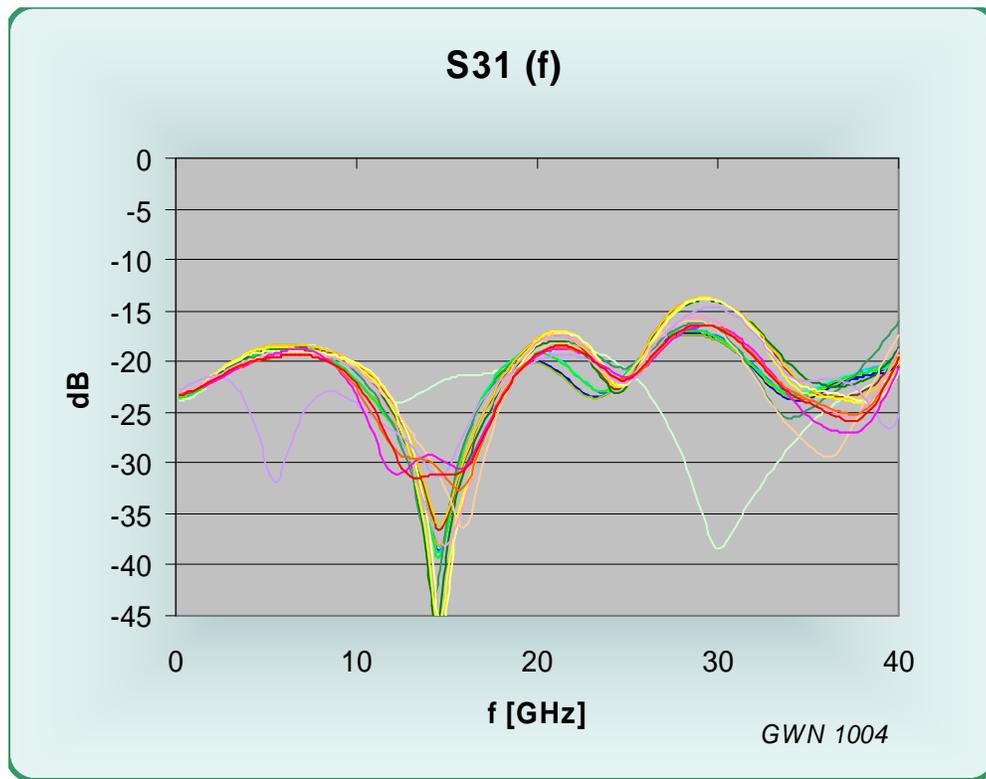

Figure 46 Crosstalk as a function of frequency

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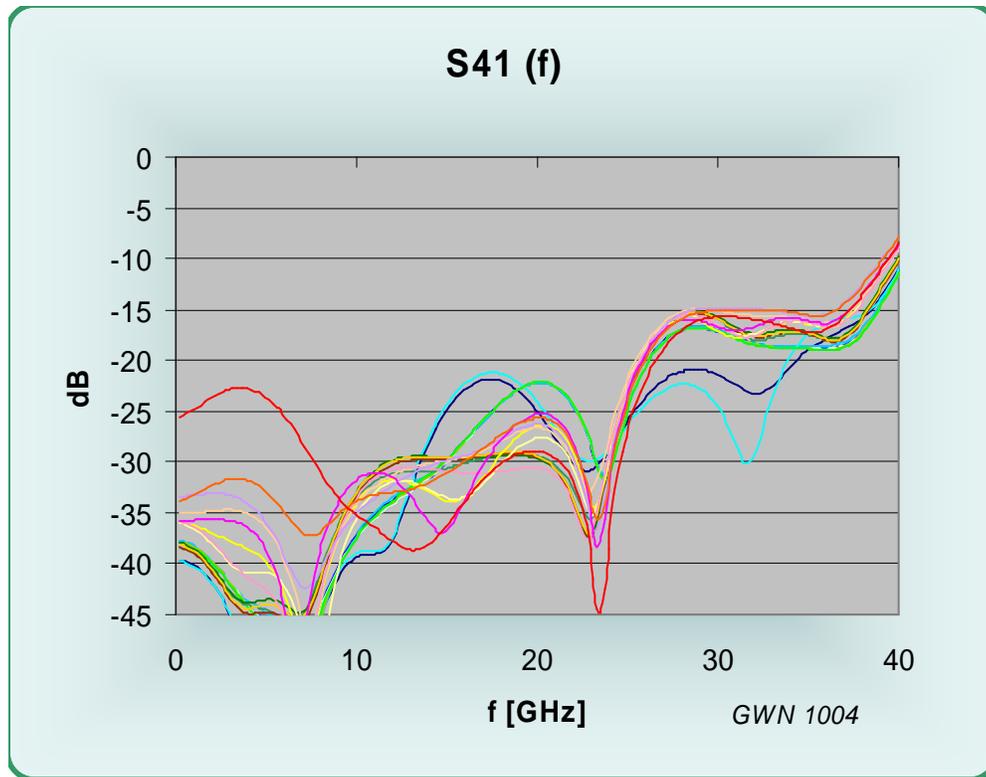
S41 (f)

GWN 1004

Figure 47 Crosstalk as a function of frequency

The graphs show forward crosstalk from port 1 to port 4 (S41) and backward crosstalk from port 1 to the adjacent terminal (port 3, S31).   Some change in intermediate cycle numbers is evident, albeit toward improvement, not deterioration.

For the completeness the open circuit and short circuit backward crosstalk S31 are also recorded. Results are shown below. No major variations are observed throughout the cycling program.
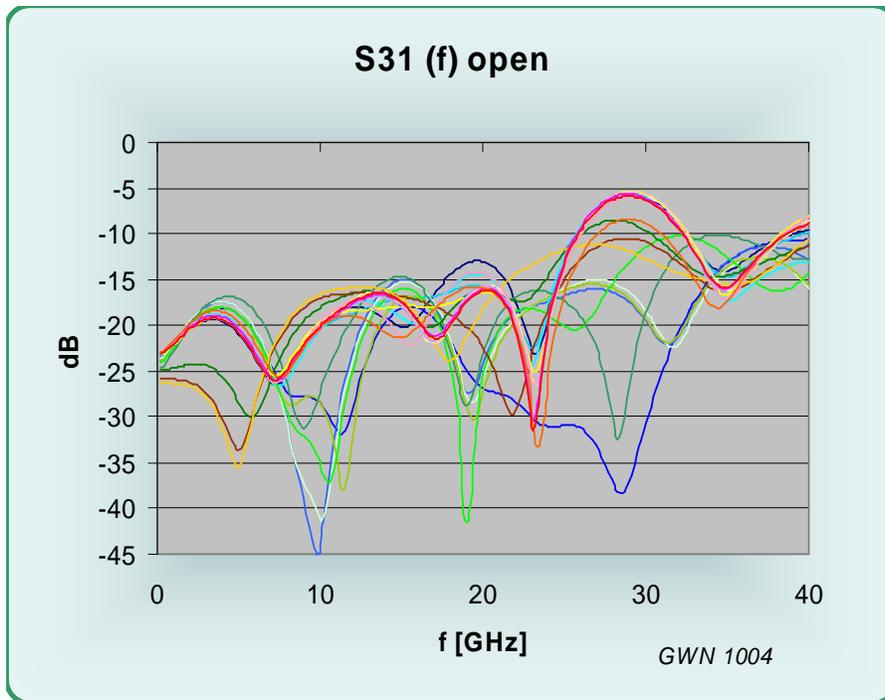
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Figure 48 Open circuit crosstalk from port 1 to port 3
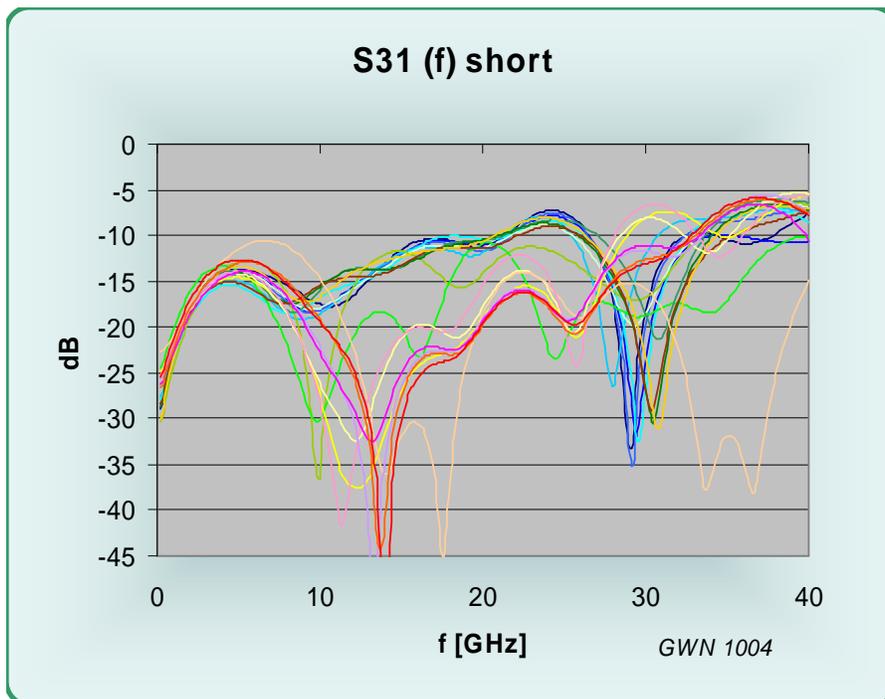
Figure 49 Short circuit crosstalk from port 1 to port 3

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Cycle chart

Shown below is a listing of the number of surrogate device insertion cycles the sockets were subjected to as a function of the sequence number. Surrogate devices were exchanged after each sequence (or 100,000 cycles, whichever is less):

1	0
2	0
3	0
4	0
5	8192
6	8192
7	8192
8	8192
9	65536
10	65536
11	65536
12	65536
13	262144
14	262144
15	262144
16	262144
17	1048576
18	1048576
19	1048576
20	1048576

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Appendix

To verify the potential impact from the formation of parasitic transmission lines, a SPICE model was established that demonstrates insertion loss response in the presence of a short circuited coupled parasitic transmission line:
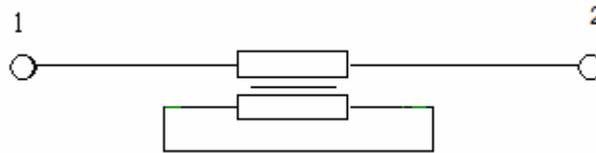
A discretized model yielded the following insertion loss simulation result:
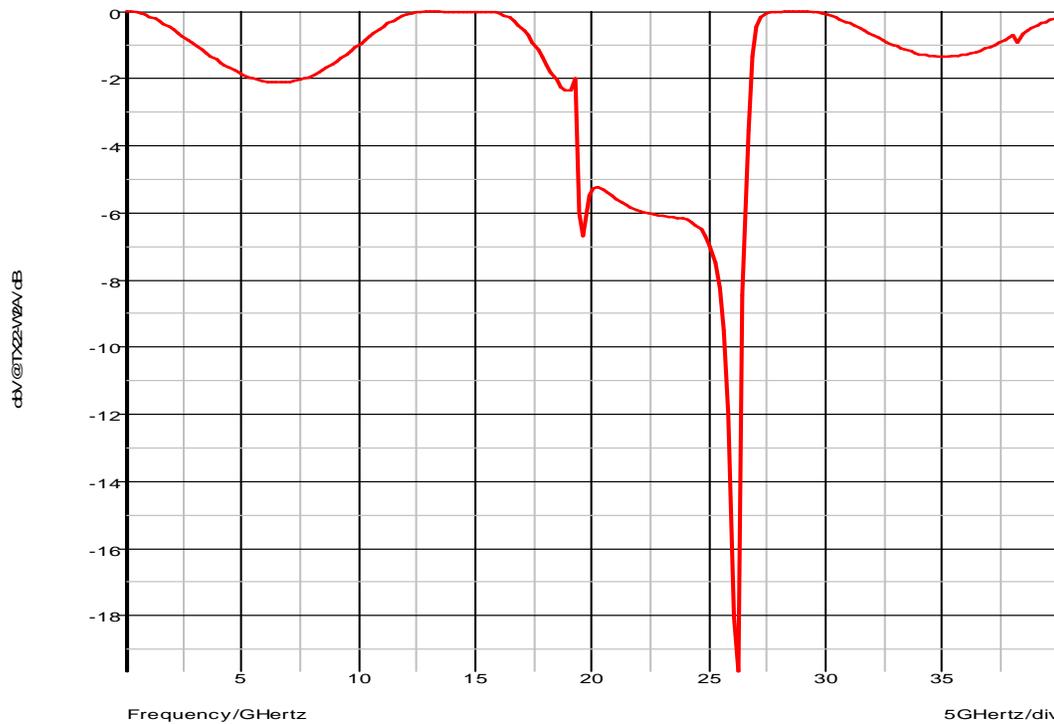
Resemblance to actual results is apparent. No further attempts were made to quantify the impact and details.

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