

Aries

0.4 mm Socket Test and Model Results



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GateWave Northern, Inc.

6200 Gisholt Dr. Ste. 205
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Objective

- Test socket
 - Return loss (S_{11})
 - Insertion loss
 - Impedance



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Setup

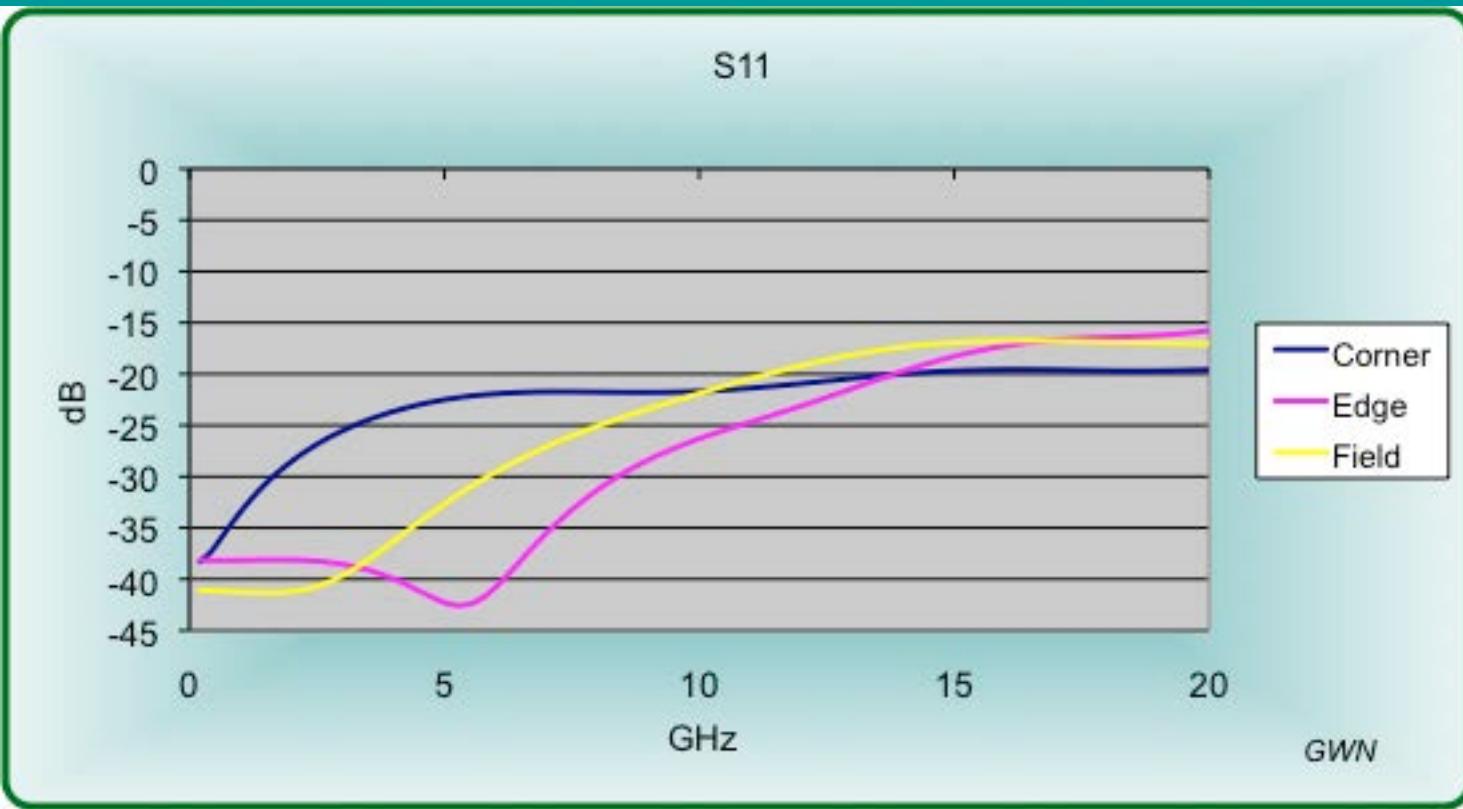
- Agilent HP8722C VNA option 10
 - 50 MHz-40.05 GHz
 - Effective risetime ~ 25 ps
 - Custom probes
-
- ANSYS HFSS 3D field modeler



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Return loss S11 measured



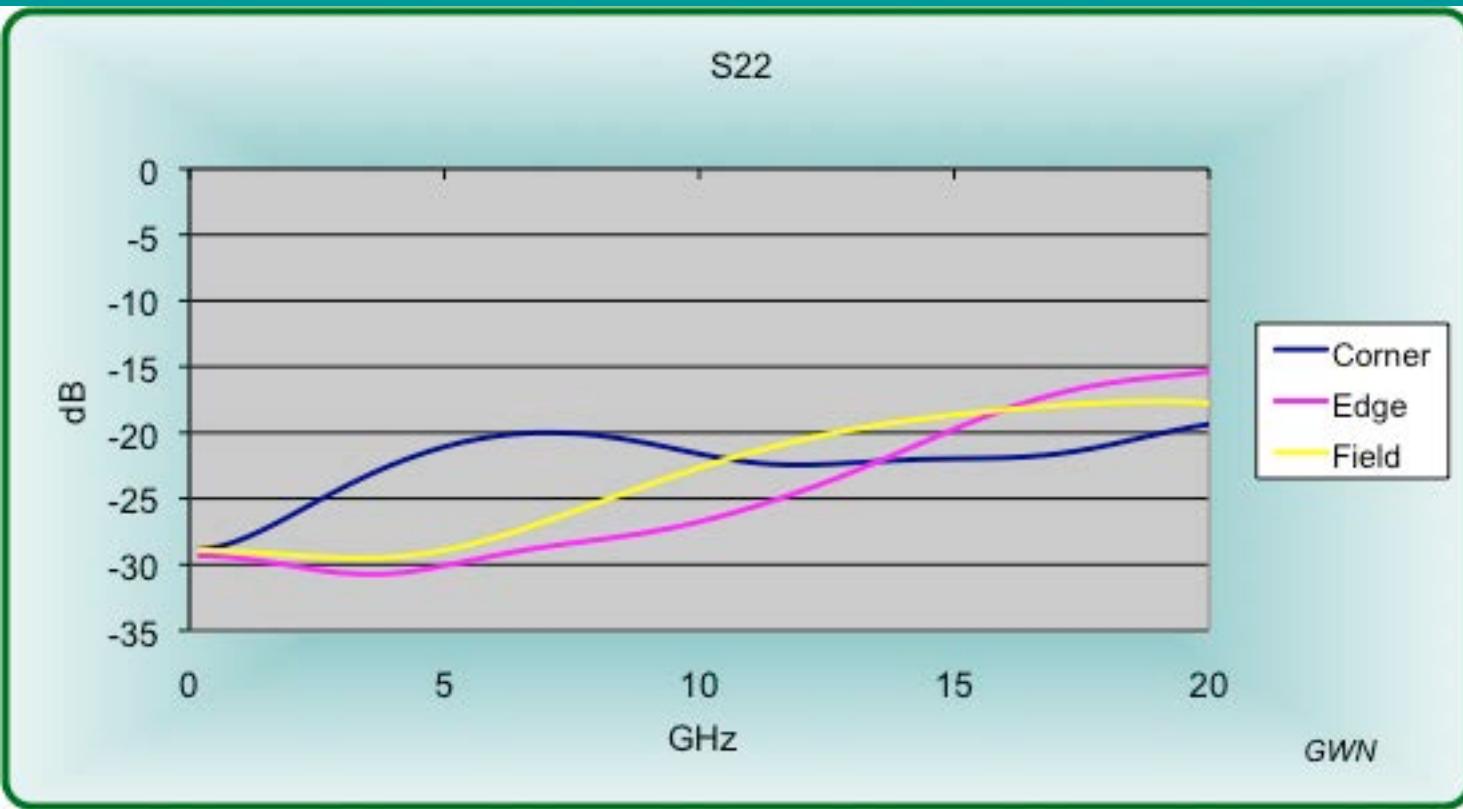
Return loss from PCB side



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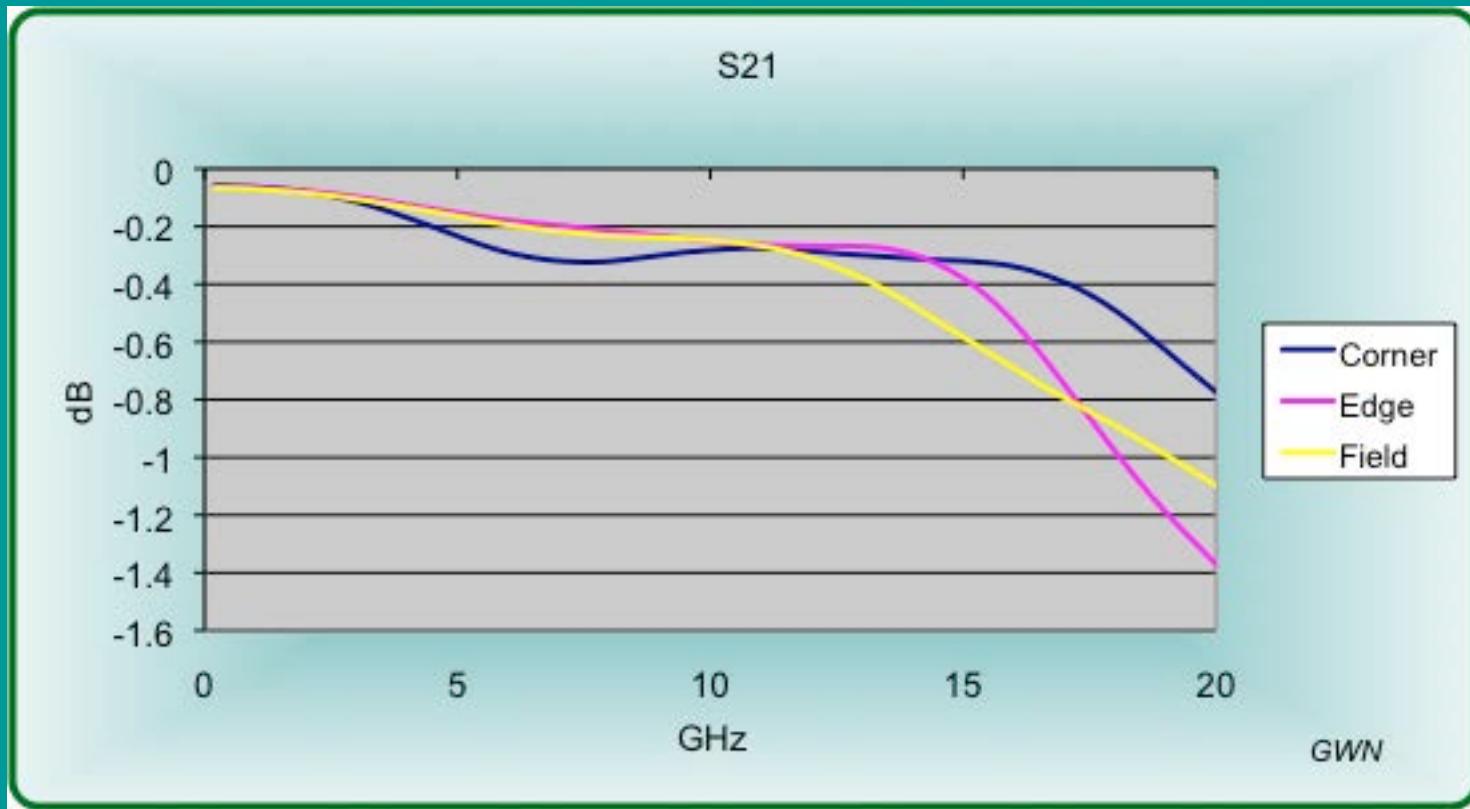
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Return loss S22 measured



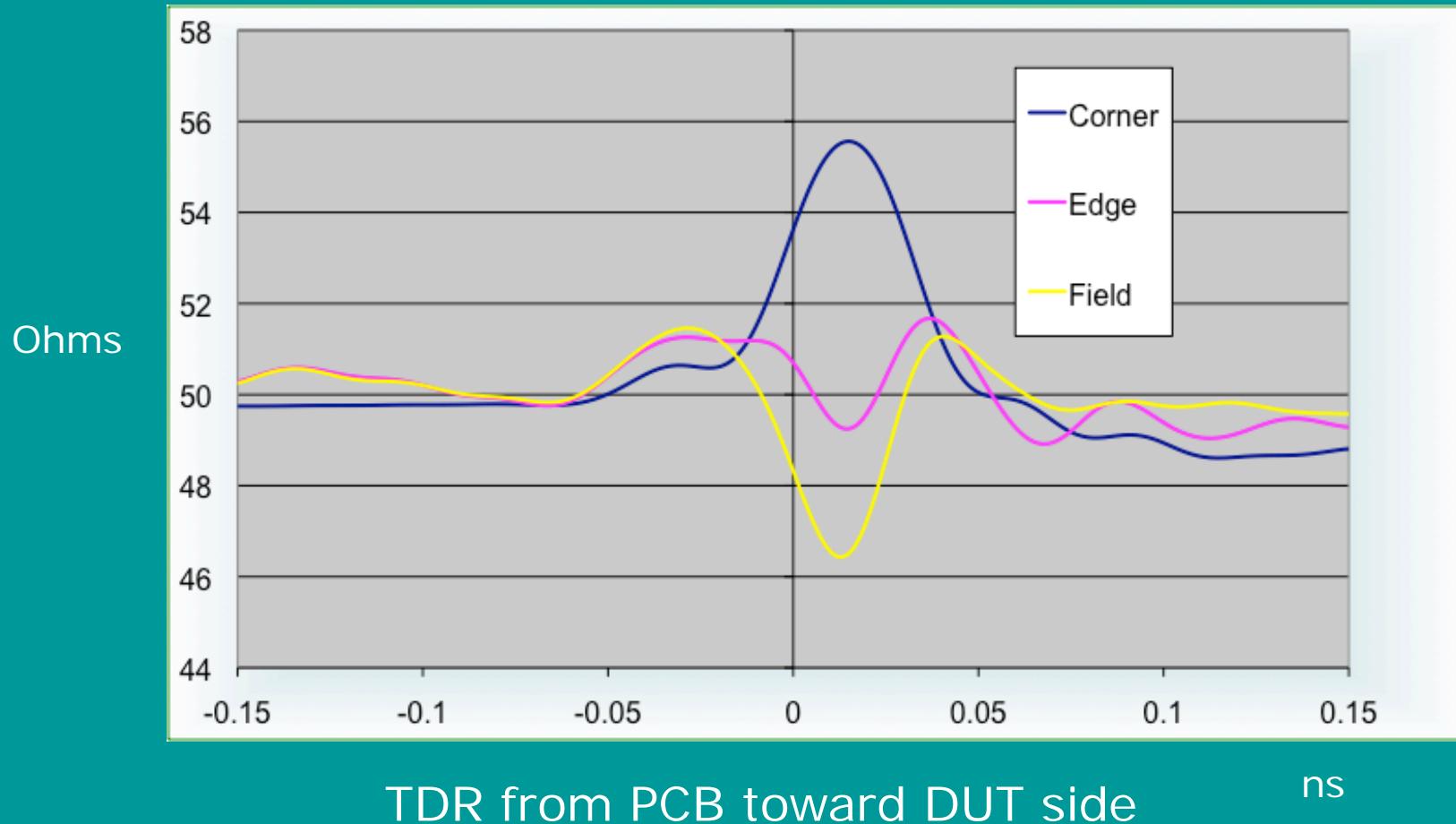
Return loss from DUT side

Insertion loss S21 measured

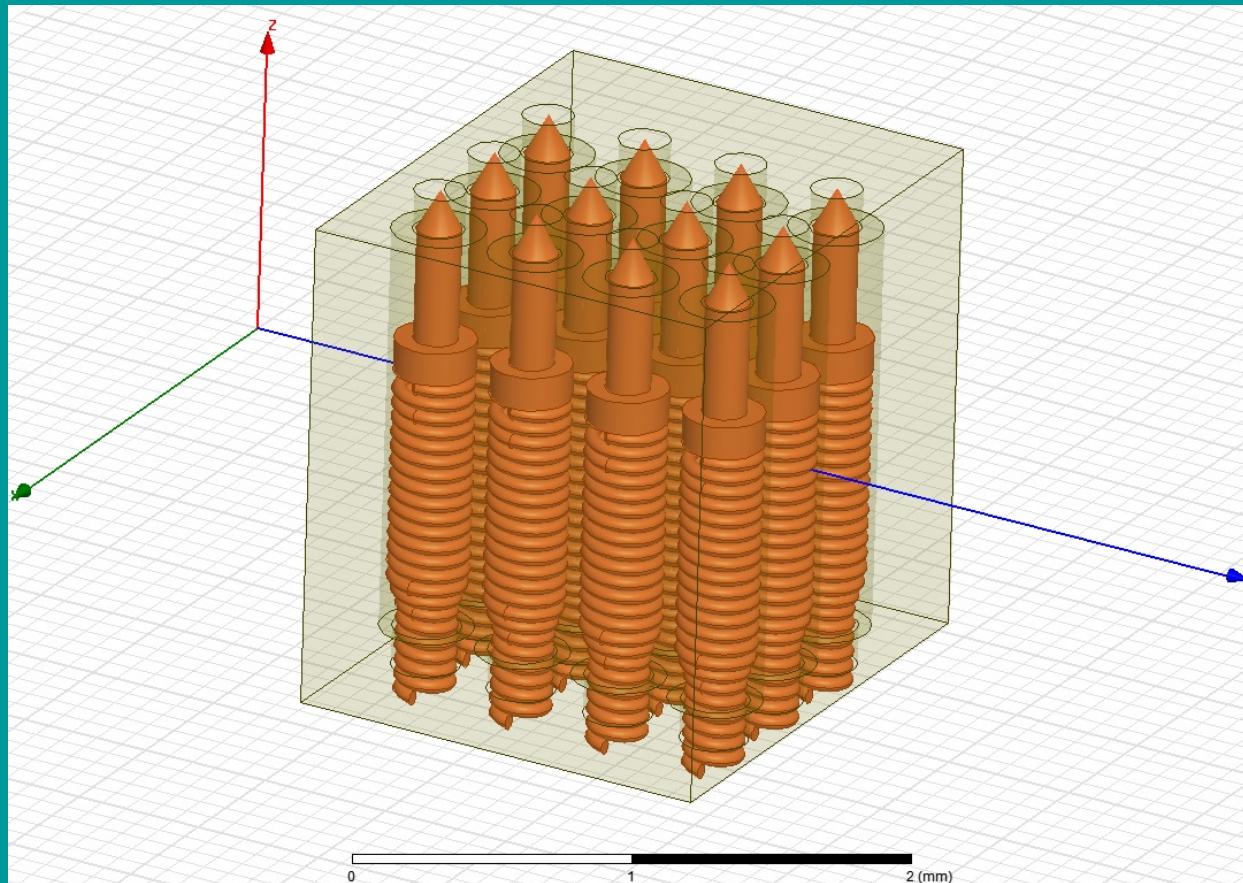


Insertion loss from PCB to DUT side

Impedance measured



HFSS model



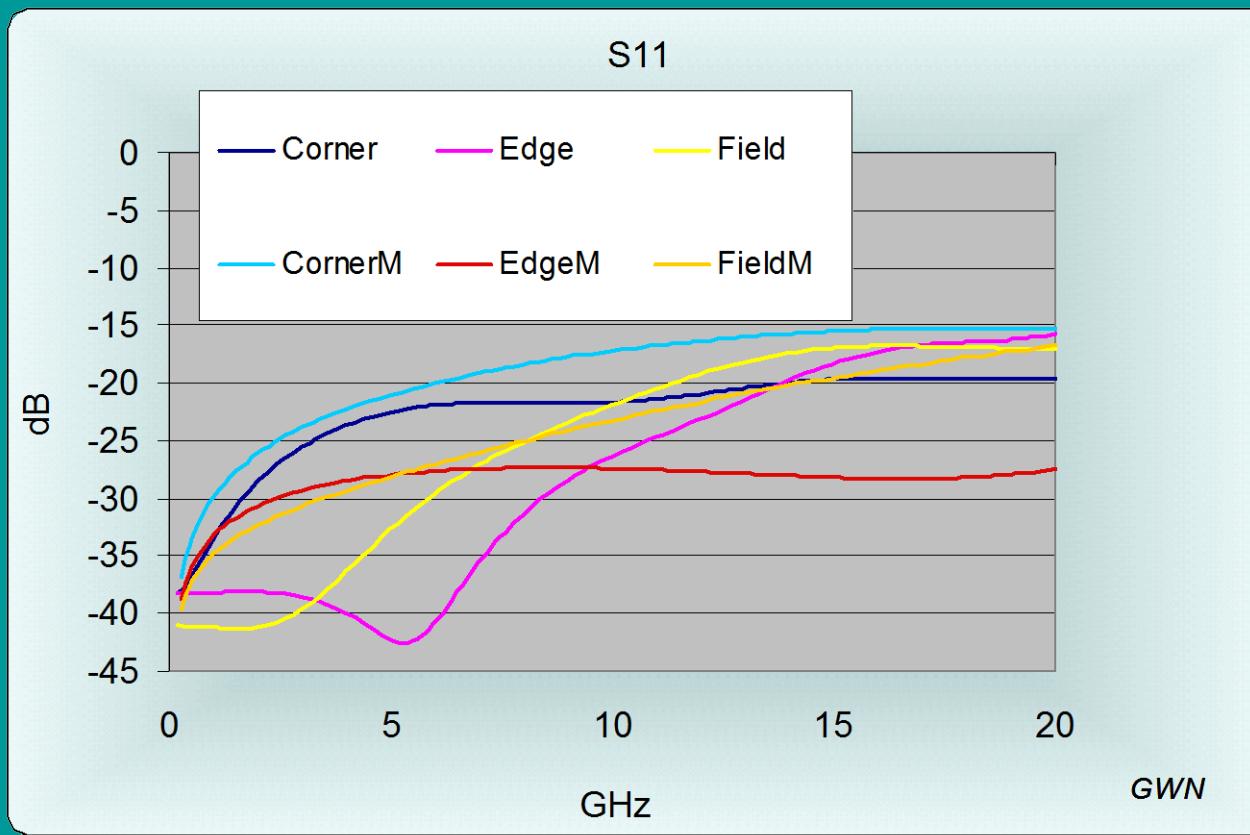
3x4 array for 3D model



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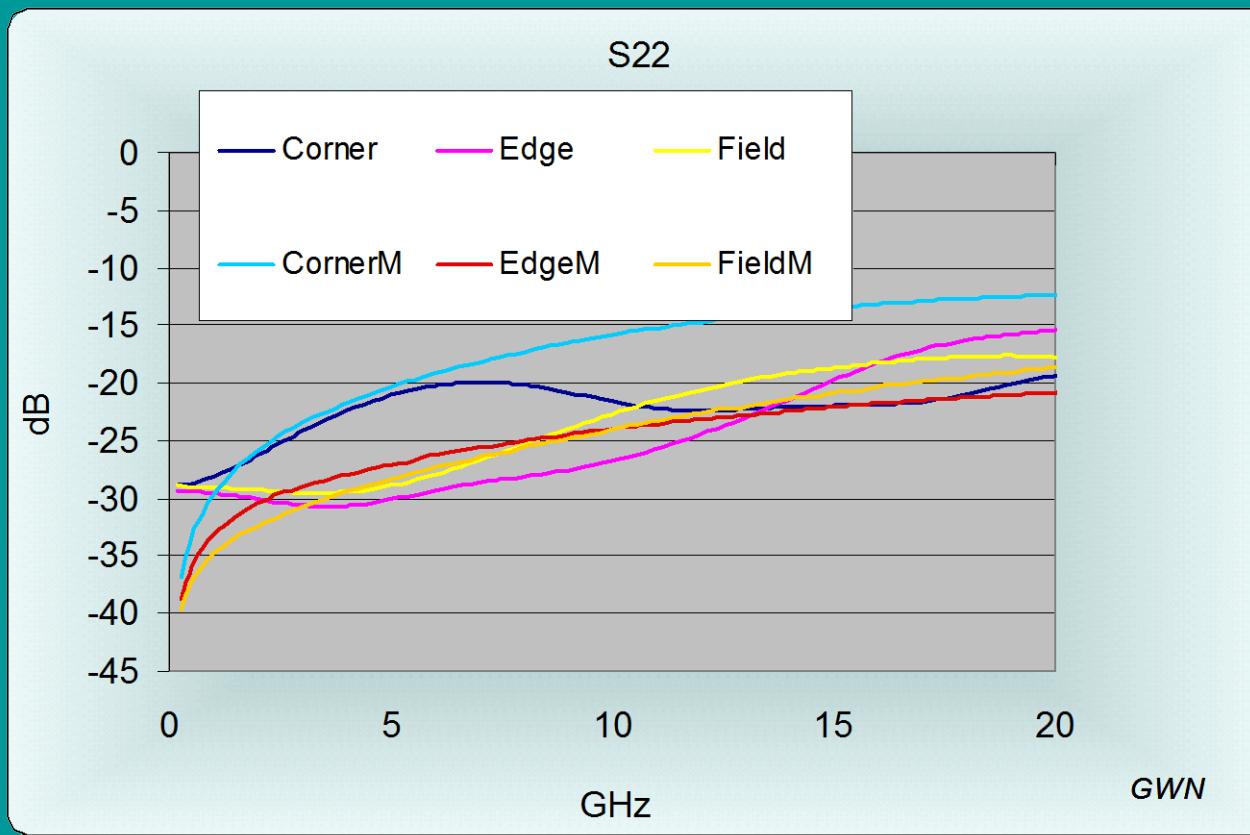
Return loss S11



Return loss from PCB side – 'M' = model

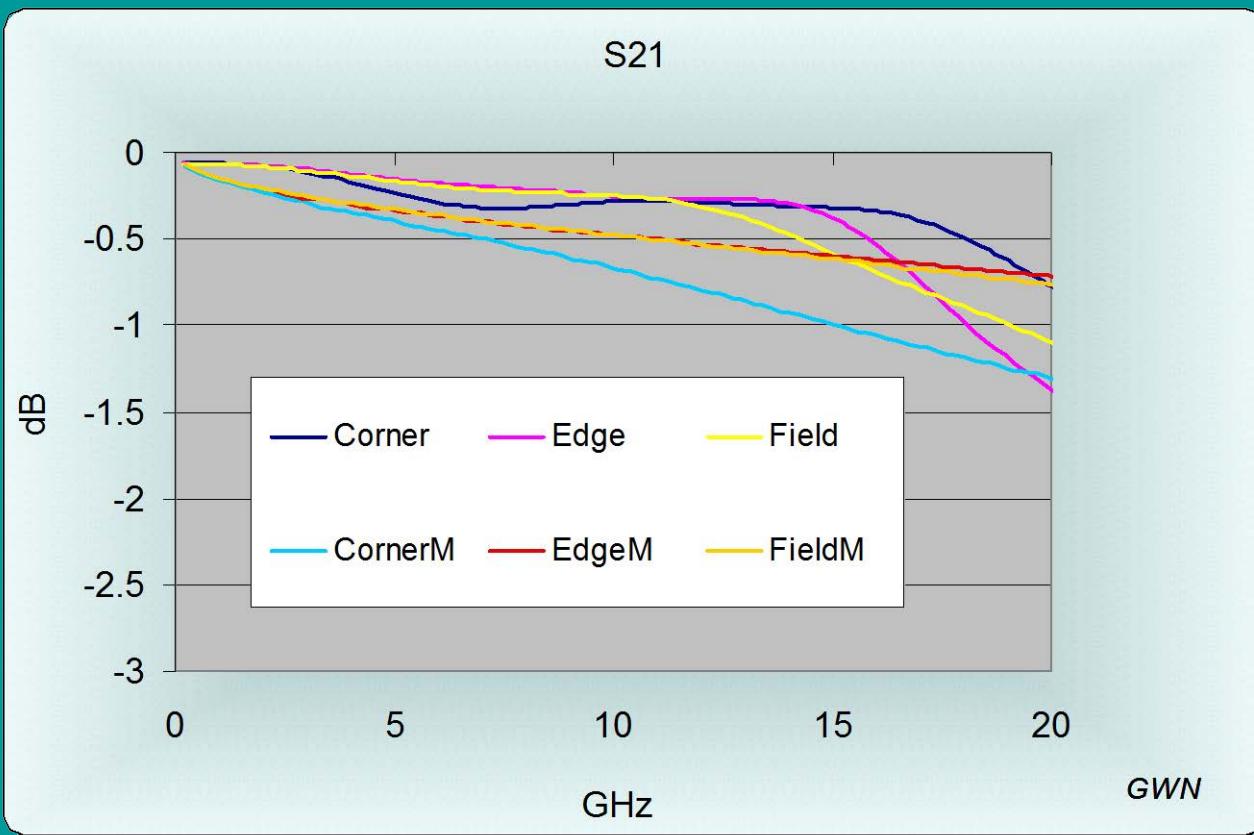


Return loss S22



Return loss from DUT side- 'M' = model

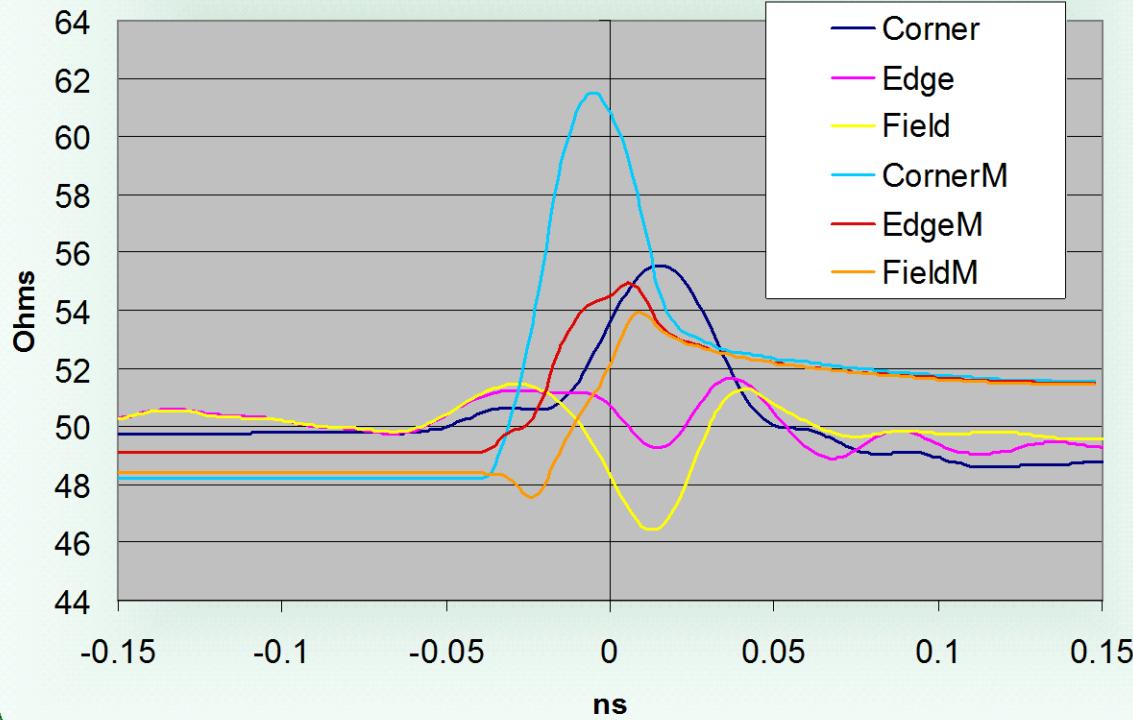
Insertion loss S21



Insertion loss from PCB to DUT side – 'M' = model

Impedance

TDR



TDR from PCB toward DUT side

'M' = model (risetime is faster than measurement and will lead to higher peaks)



Summary

- Return loss performance is best for the edge case since impedance is closest to 50 Ohms in that configuration
- There is reasonable agreement between model and measurement up to about 10 GHz.
- It appears a few coils never close completely. This introduces some uncertainty in the model as their number is not known.

