Aries
Center probe CSP socket
Cycling test

RF Measurement Results

prepared by

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Objective

The objective of these measurements is to determine the changes in RF performance of an Aries center probe CSP socket as it is subjected to a cycling regimen. The measurements are performed as in the individual characterization, i.e. for G-S-G configurations, a signal pin surrounded by grounded pins is selected for the signal transmission. For G-S-S-G configurations, two adjacent pins are used to transmit signals. All other pins are grounded. Measurements in both frequency and time domain form the basis for the evaluation. Parameters to be determined are pin capacitance and inductance of the signal pin, the propagation delay, and the attenuation to 40 GHz.

Methodology

Cycling of the sockets is performed according to a prescribed binary sequence. A socket is characterized after 0, 8192, 65536, 262144 and 1048576 insertions of a surrogate device. After each sequence, the surrogate device is exchanged. This means that a surrogate device may be inserted repeatedly for a large number of cycles, especially later in the test. While not entirely corresponding to an actual test situation, this approach minimizes the number of surrogate devices required and does not depend on the construction and availability of any specialized handlers.

Capacitance and inductance for the equivalent circuits were determined through a combination of measurements in time and frequency domain. Frequency domain measurements were acquired with a network analyzer (HP8722C). The instrument was calibrated up to the end of the 0.022" diameter coax probe. The probe was then connected to the fixture and the response measured from one side of the array. When the pins terminate in an open circuit, a capacitance measurement results. When a short circuit compression plate is used, inductance can be determined.

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Time domain measurements are obtained via Fourier transform from VNA tests. These measurements reveal the type of discontinuities at the interfaces plus contacts and establish bounds for digital system risetime and clock speeds.

The focus of this test was stability and repeatability. Deviations from the actual characterization of the device as reported in the cycle 0 test reports may therefore be apparent. This was tolerated in the interest of interchangeability and uniformity of testing since the test setup and procedures were simultaneously used for a number of different sockets.

Test procedures

To establish capacitance of the signal pin with respect to the rest of the array, a return loss calibration is performed. Phase angle information for S11 is selected and displayed. When the array is connected, a change of phase angle with frequency can be observed. It is recorded and will be used for determining the pin capacitance.

The self-inductance of a pin is found in the same way, except the center probe CSP socket contact array is compressed by a metal plate instead of an insulator. Thus a short circuit at the far end of the pin array results. Again, the analyzer is calibrated and S11 is recorded. The inductance of the connection can be derived from this measurement.

Setup

The setup used for the cycling consists of a small mechanical device with two parallel plates (see Fig.1). The plate spacing of this cycler varies periodically and is adjustable to a rate of up to 3 cps. Overdrive conditions are adjusted with shims according to the requirements of the individual socket. A presettable counter controls the number of test cycles.

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Figure 1 DUT cycling station

Testing was performed with a test setup that consists of a brass plate that contains the coaxial probes. The DUT is aligned and mounted to that plate. The opposite termination is also a metal plate with coaxial probes, albeit in the physical shape of an actual device to be tested.   Fig. 2 shows a typical arrangement of base plate and DUT probe:
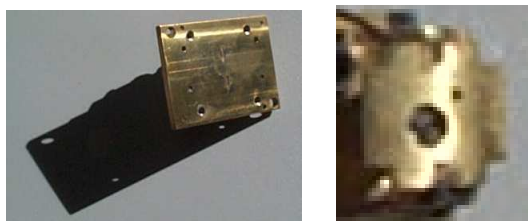

Figure 2 DUT mounting plate and DUT test plate

For cycling, the socket is mounted on a brass plate with Au over Ni coating equivalent to that found on PCBs. This plate also provides for insertion of a DC test probe for DC measurements.

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After the prerequisite number of surrogate device insertions, the socket is transferred to the RF test base plate for characterization. The center probe CSP socket and base plate as well as the DUT plate are then mounted in a test fixture as shown below in Fig. 3:
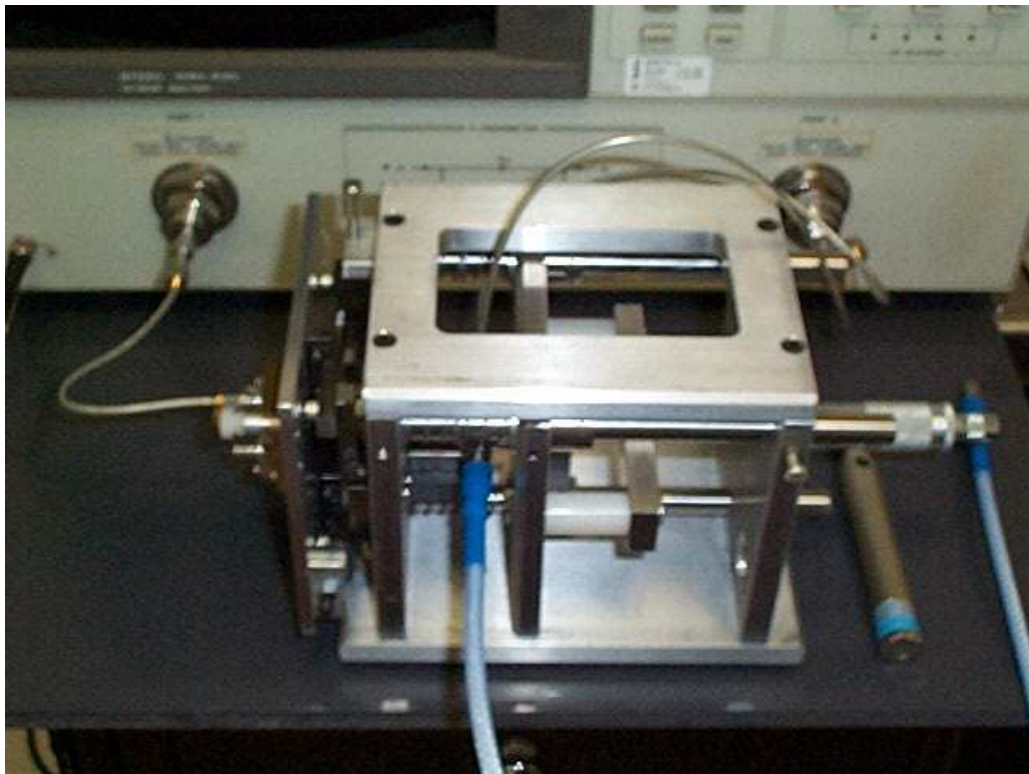

Figure 3 Test fixture

This fixture provides for independent X, Y and Z control of the components relative to each other. X, Y and angular alignment is established once at the beginning of a test series and then kept constant. Z alignment is measured via micrometer and is established according to specifications for the particular DUT. Connections to the VNA are made with high quality coaxial cables with K connectors.

After RF characterization, the socket is transferred back to the dc test plate for further cycling.

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For G-S-S-G measurements, the ports are named as follows:
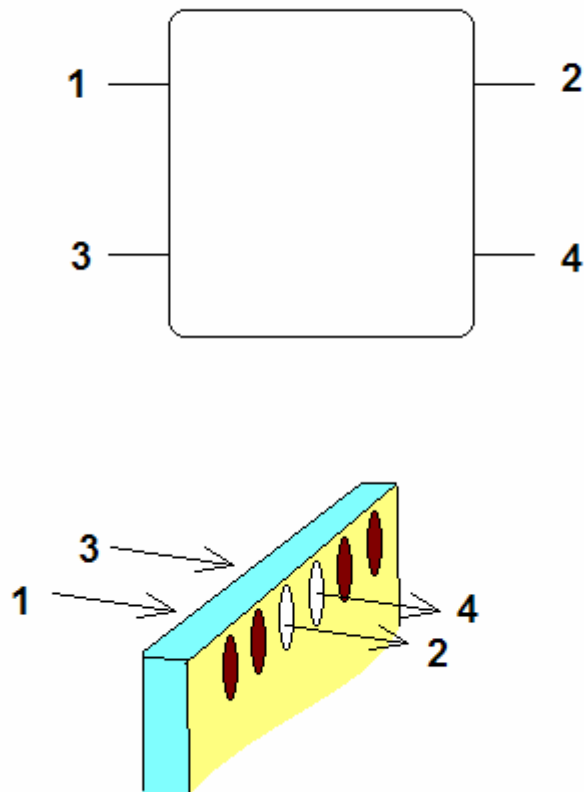
Figure 4 Ports for the G-S-S-G measurements

Signals are routed though two adjacent connections (light areas), unused connections are grounded (dark areas).

It should be noted that the port naming convention used here deviates from the traditional port assignments to be compatible with the existing data acquisition software.

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Measurements G-S-G

Time domain

The time domain measurements will be presented first because of their significance for digital signal integrity. TDR reflection measurements (and the corresponding color key) are shown in the following graphs:
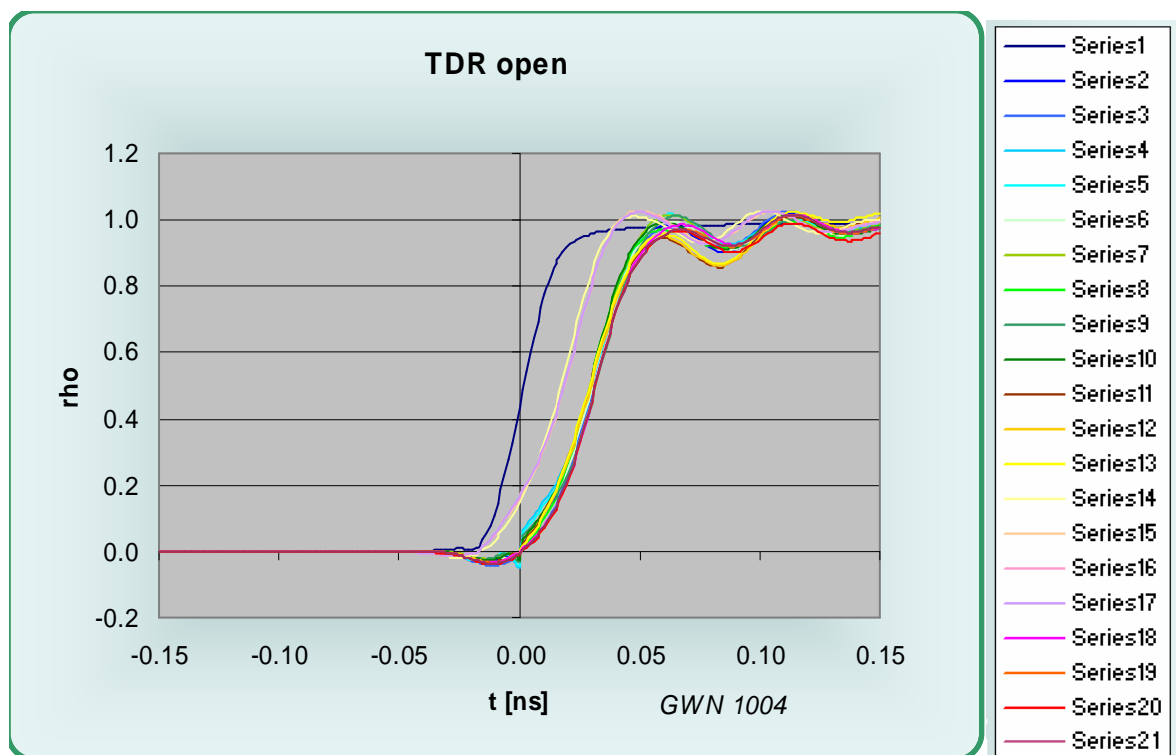
Figure 5 TDR signal from an OPEN circuited center probe CSP socket

The reflected signals from the center probe CSP socket (rightmost traces) show some deviation in shape from the original waveform (leftmost trace). The average risetime is 43.0 ps and is only slightly larger than that of the system with the open probe (28.5 ps). The risetime standard deviation is 17.8 ps throughout the sequence of tests.

Average electrical pin length is 12.6 ps one way with a standard deviation of 2.4 ps.

Statistical data was extracted from the datasets at each particular point in time.

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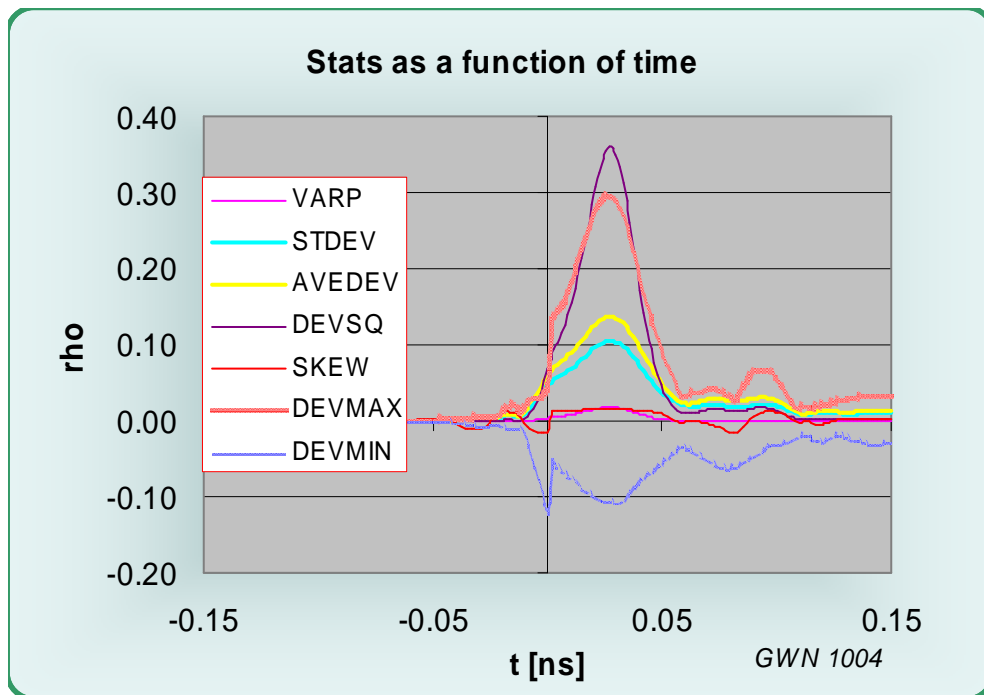
Figure 6 TDR signal from an OPEN: Statistics

   More detail about the individual statistics can be found in the dc test report (cycling) and MSExcel. The maximum and minimum deviations from the average values are also shown (DEVMAX and DEVMIN = error bands).

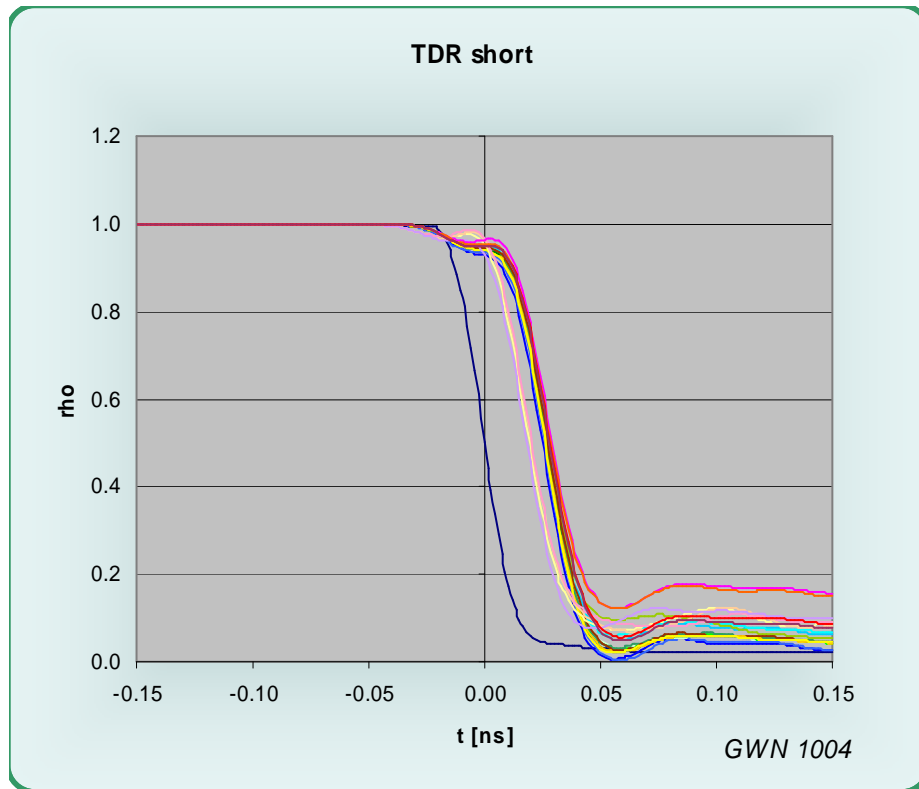   Not surprisingly, values peak in the transition region.

Figure 7 TDR signal from a SHORT circuited center probe CSP socket

For the short circuited center probe CSP socket the average fall time is 44.2 ps with a standard deviation of 31.7 ps. This is a small increase over the system risetime of 25.5 ps. The average electrical length for this case is 12.9 ps with a standard deviation of 1.6 ps.

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Statistics for the short circuit response datasets yield the following results:
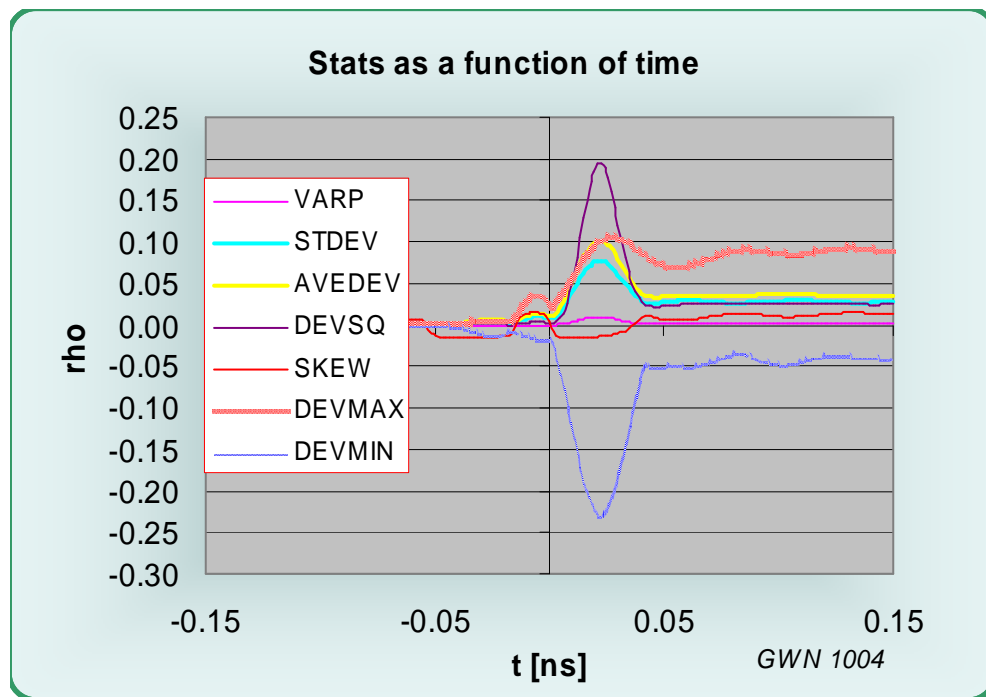
Figure 8 Short circuit dataset statistics

TDR thru

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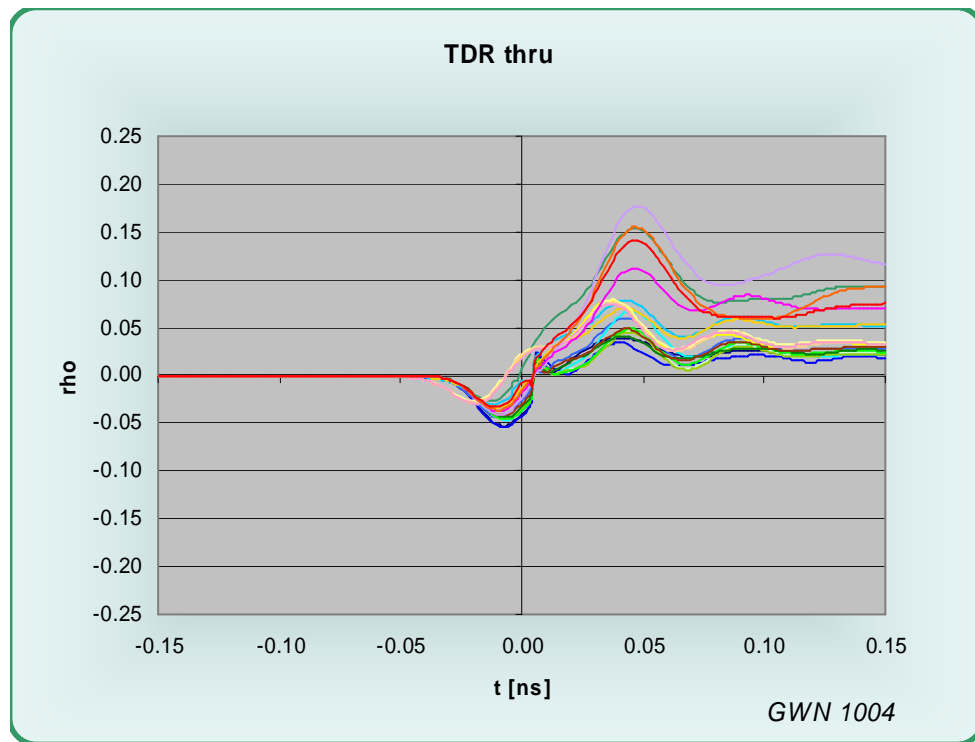
Figure 9 TDR measurement into a 50 Ohm probe

The thru TDR response shows both inductive and capacitive responses. The high peak average corresponds to a transmission line impedance of 59.1 Ohms, the low peak average (dip to negative values) to 46.3 Ohms. The standard deviations are 5.4 Ohms and 0.8 Ohms, respectively. The dip is possibly caused by fixture pad's presence to the socket material, which causes capacitive loading. When graphed, the following dependence of the peak on cycle number is obtained:

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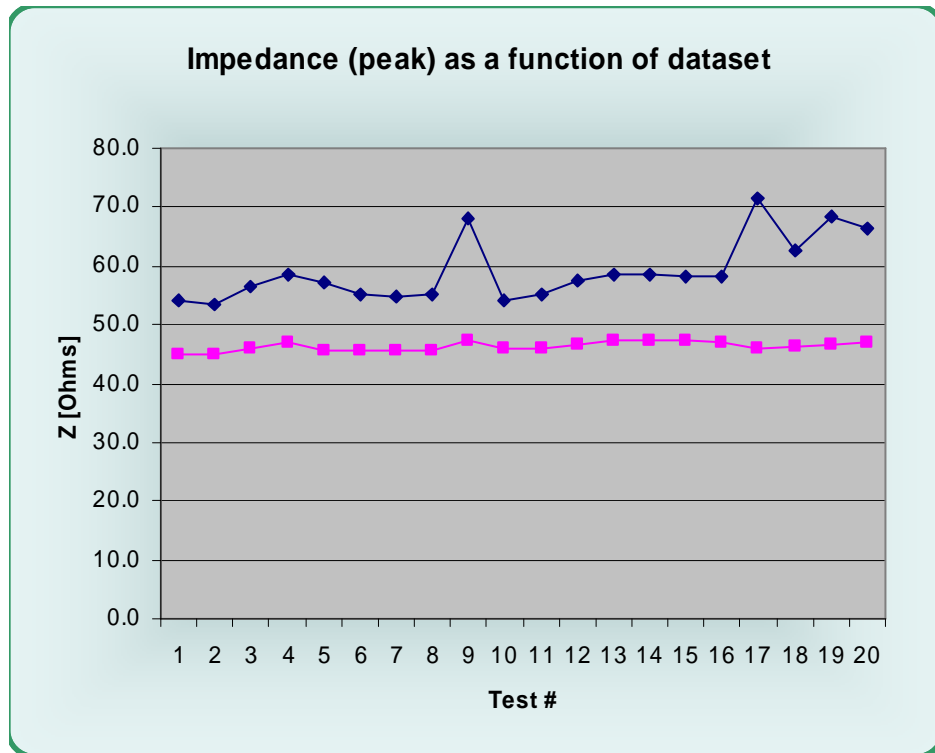
Figure 10 Thru impedance peaks as a function of cycle #

The TDT performance for a step propagating through the pin arrangement was also recorded:

TDT
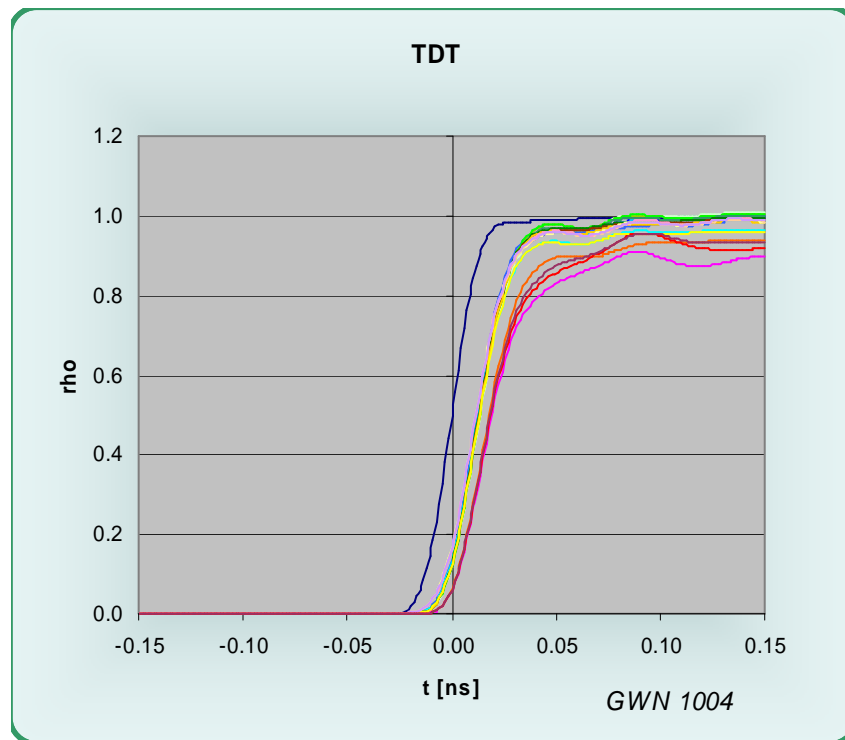
Figure 11 TDT measurement

The TDT measurements for transmission show a small contribution to risetime from the pin array (average 10-90% RT = 33.6 ps @ 2.8 ps STD DEV, the system risetime is 25.5 ps). The average added delay at the 50% point 13.5 ps with a standard deviation of 1.9 ps. There is no significant signal distortion.

The chart of the risetime as a function of cycle number shows no significant change with the number of test sequences except for the 1 million cycle mark:

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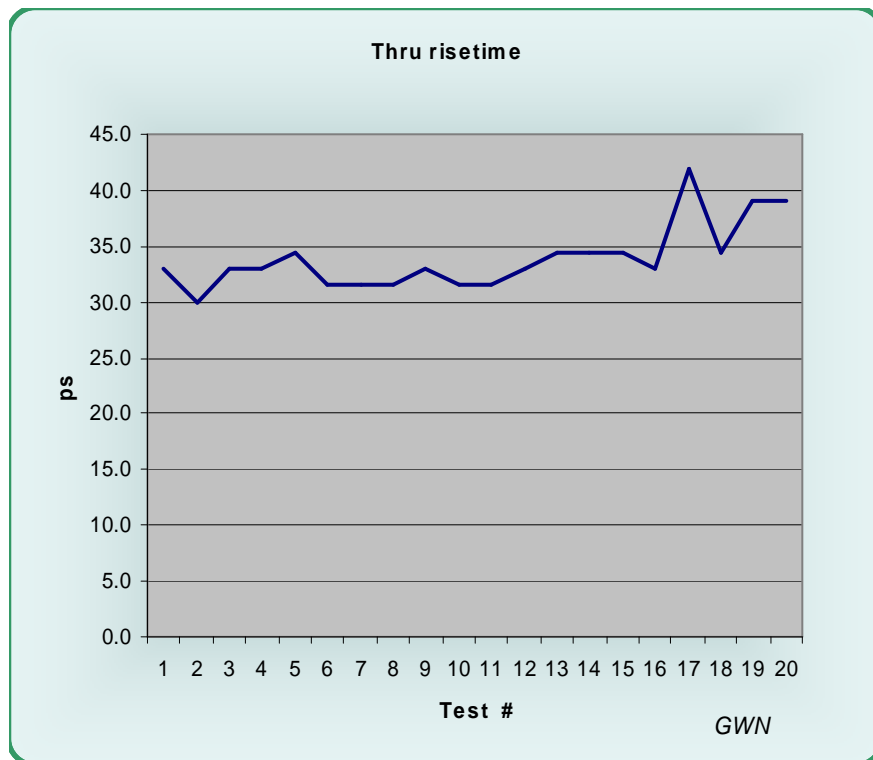
Figure 12 TDT risetime as a function of cycle number

Frequency domain

Network analyzer reflection measurements for a single sided drive of the signal pin with all other pins open circuited at the opposite end were performed to determine the pin capacitance. The analyzer was calibrated to the end of the probe and the phase of S11 was measured. From this curve the capacitance of the signal contact to ground can be determined (see below).
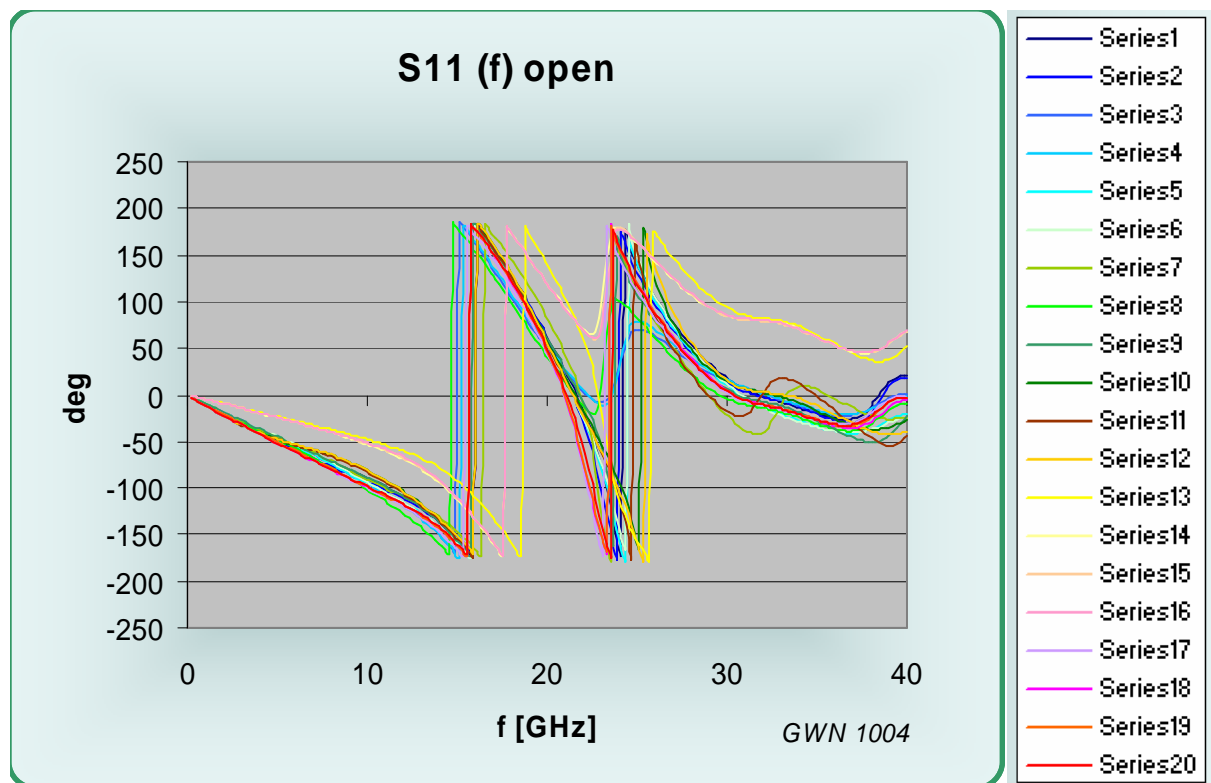

Figure 13 S11 phase (f) for the open circuited signal pin

A number of cycles show smaller phase changes than the majority. Deviations indicate a less capacitive behavior. All occurred in the sequence of tests after 250,000 cycles. As will be seen, other parameters were affected as well. The cause of this is not clear. It is, in principle, possible that a particle was trapped under the socket, altering the properties of the connection. Another possibility is a change in the test setup. This was not reflected in the results of two other sockets tested concurrently, however. Properties returned to their previous values after 1 million cycles.
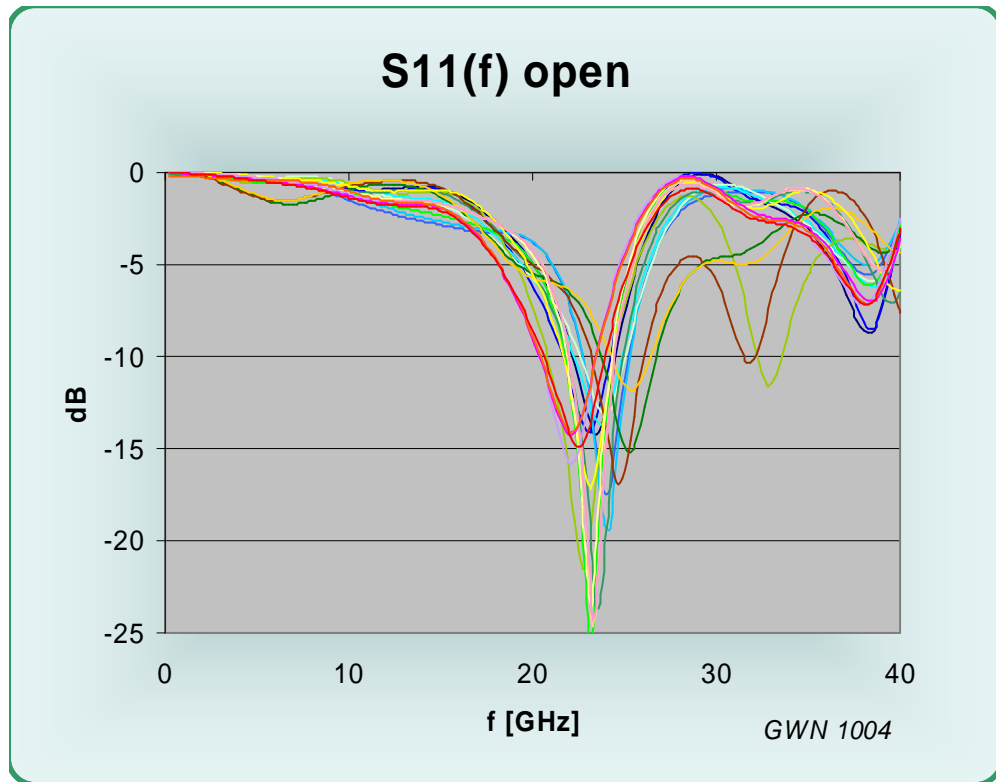
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Figure 14 S11 magnitude (f) for the open circuited signal pin

While ideally the magnitude of S11 should be unity (0 dB), loss, radiation and resonances in the array are likely contributors to noticeable return loss for the open circuited pins at elevated frequencies. Just like in case of the phase above, some connection uncertainty due to the probe construction on the PCB side of the socket is thought to contribute to scatter of the data.

A 3D representation of the open circuit return loss shows how this loss evolves with increasing sequence number (S1-S20):

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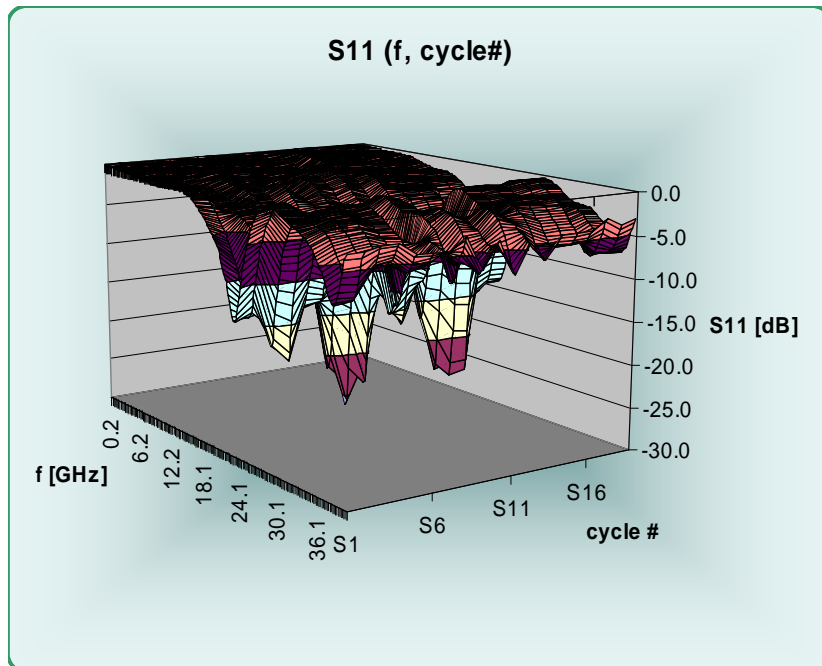
Figure 15 S11 magnitude (f) for the open circuited signal pin

Resonance conditions like the one observed at 35 GHz are particularly sensitive to small changes in the setup, the DUT and the instrument calibration. Thus deviations recorded in the datasets for each frequency (cycle1 thru 20) displayed as a function of frequency (definitions can be found in MSExcel and the dc test report) also increase:
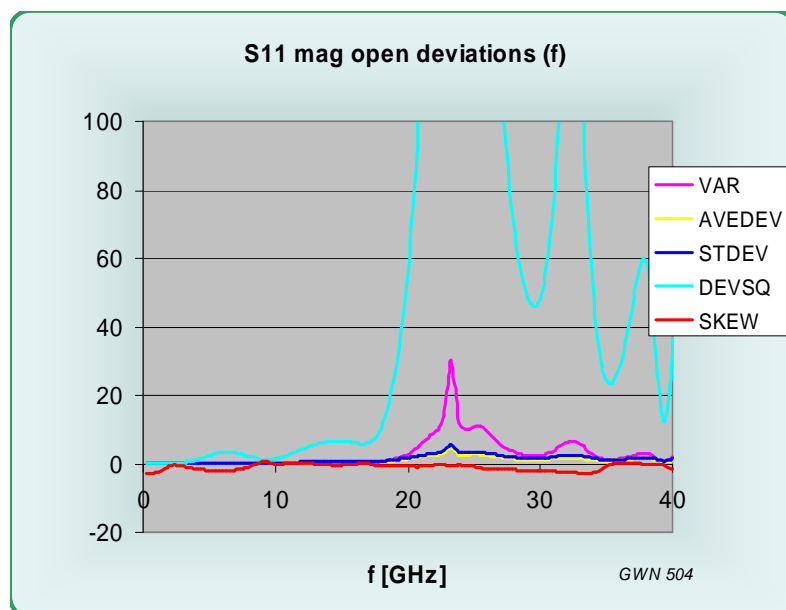

Figure 16 S11 magnitude deviations (f) for the open circuited signal pin

When calculating the capacitance of the signal pin with respect to ground from the measurements, the following results are obtained:
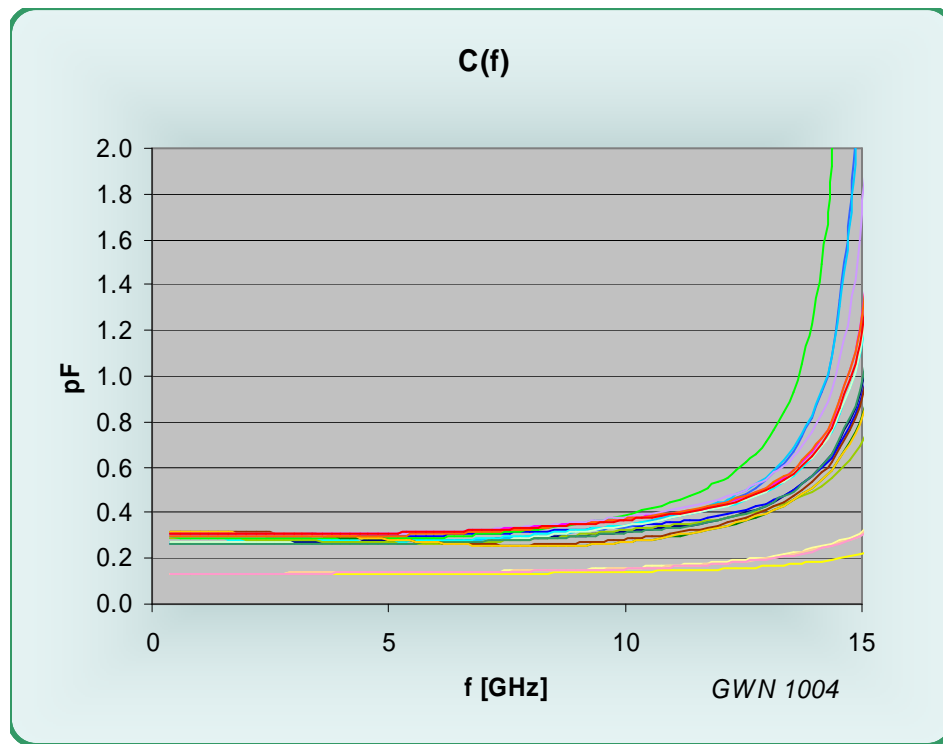
Figure 17 C(f) for the open circuited signal pin

The average capacitance is 0.26 pF at low frequencies. Standard deviation is 0.066 pF. Scatter is due to the undetermined sequence of test cycles with different results mentioned earlier.

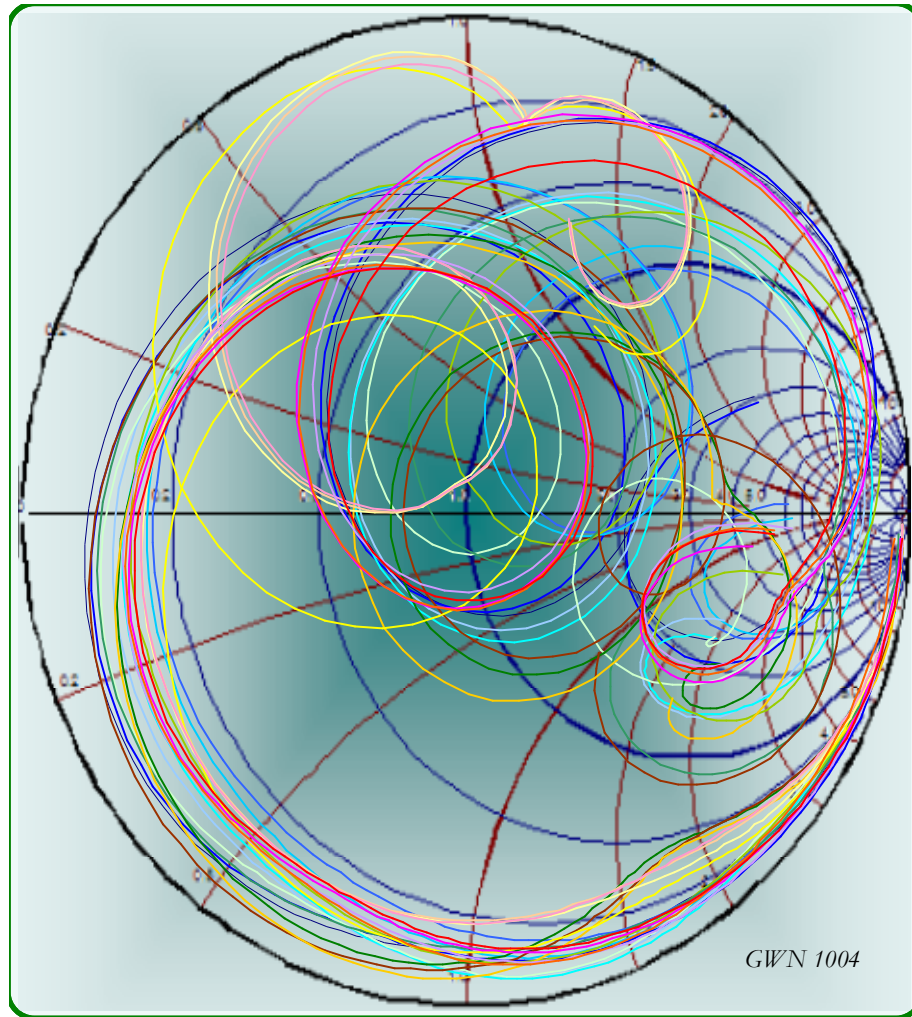The Smith chart measurement for the open circuit shows only a minute resonance toward the upper frequency limit of 40 GHz.

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Figure 18 Reflections from the open circuited center probe CSP socket

To extract the pin inductance, the same types of measurements were performed with a shorted pin array. Shown below is the change in reflections from the center probe CSP socket. Calibration was established with a short placed at the end of the coax probe. Variability at elevated frequencies is again attributed to an uncertainty in the contact point for the socket's PCB side connection (see above).
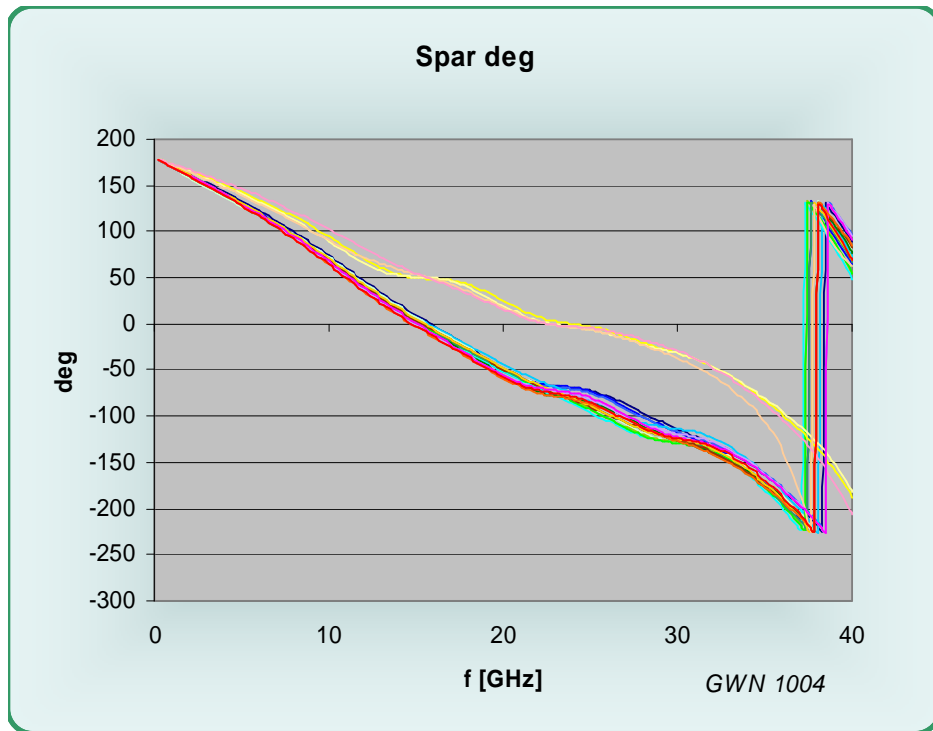
Figure 19 S11 phase (f) for the short circuited case
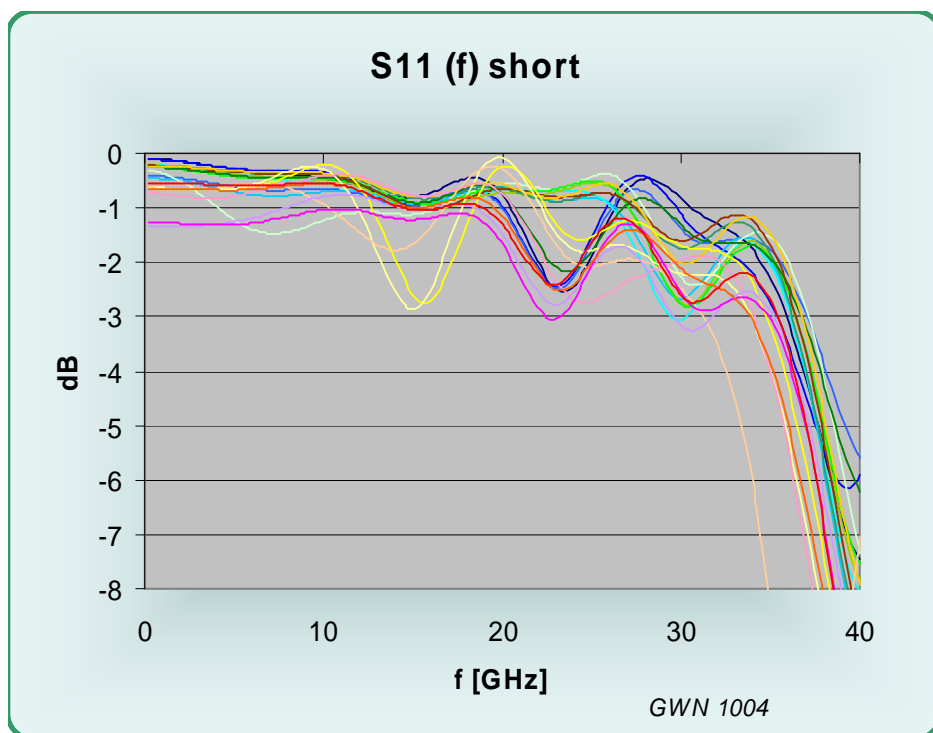
Figure 20 S11 magnitude (f) for the short circuited case

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A 3D plot reveals trends with increasing cycle numbers:
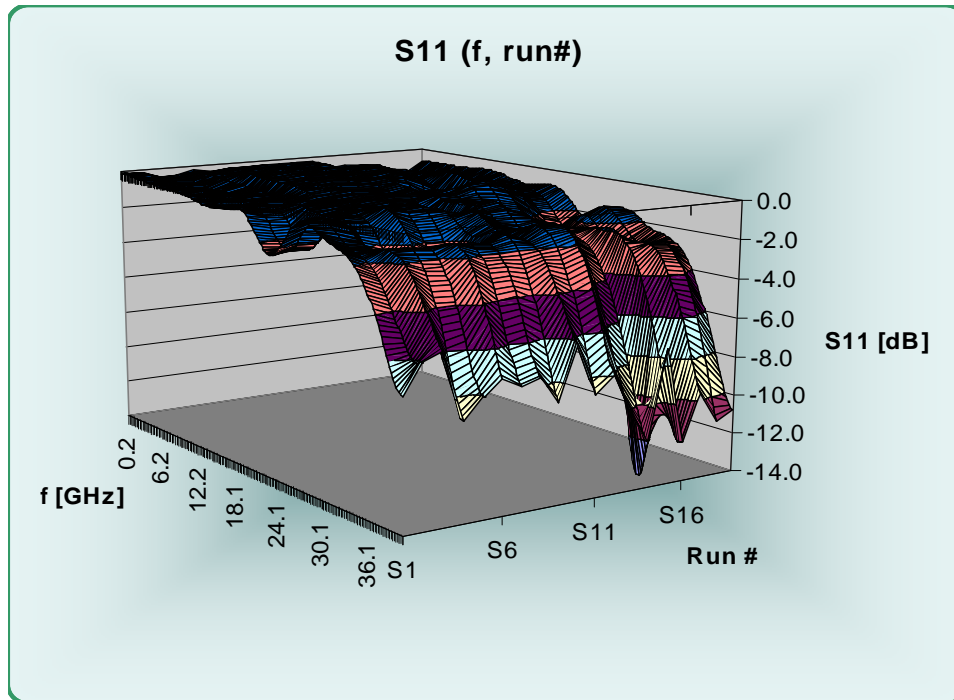

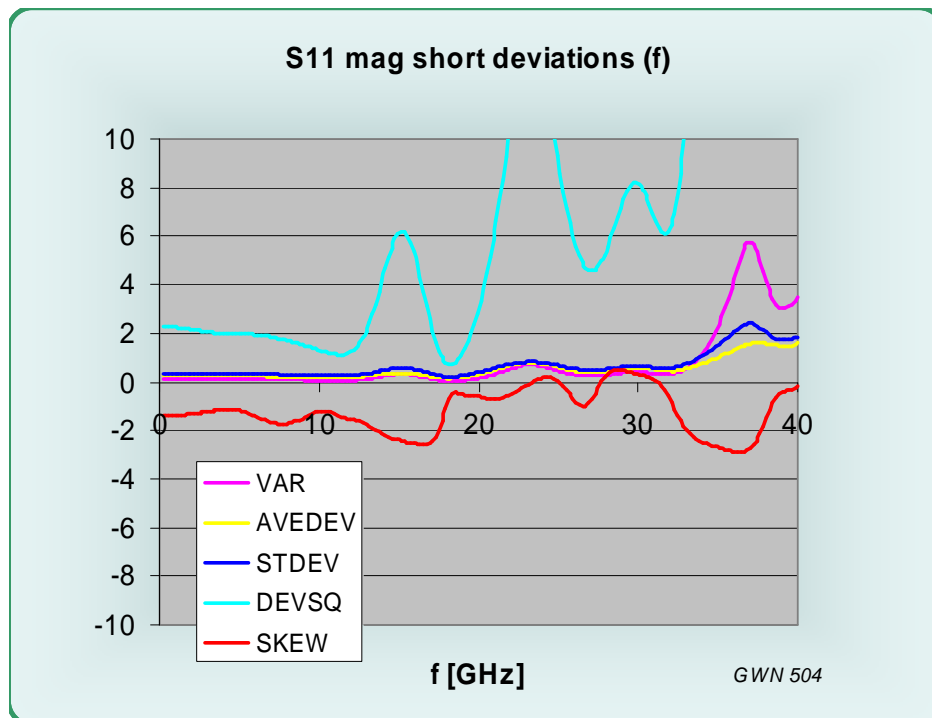Figure 21 S11 magnitude (f) for the short circuited case

Figure 22 S11 magnitude deviations (f) for the short circuited case

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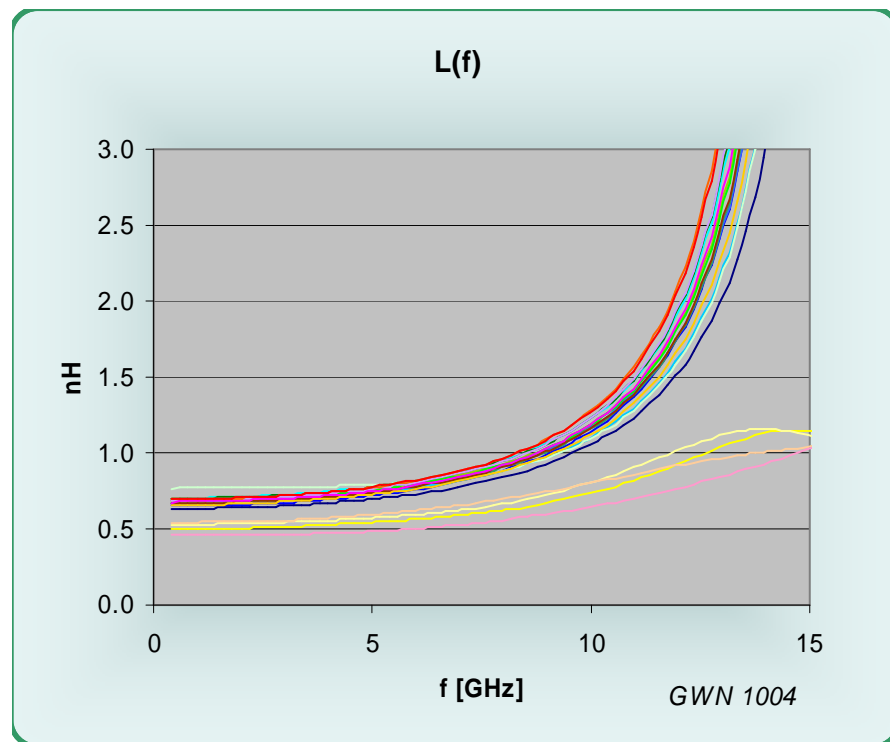From these measurements the inductance of the pin can be extracted. Its evolution with frequency is shown below:

L(f)

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Figure 23 L(f) for the center probe CSP socket

The phase changes recorded correspond to an average inductance of 0.65 nH at low frequencies. A standard deviation of 0.08 pH exists.   The inductance rise toward 15 GHz is likely due to the fact that the pins form a transmission line with a length that has become a noticeable fraction of the signal wavelength.

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While there is some variation, the overall properties of the socket under test for the short circuit condition are stable as witnessed by the display of S11 in the Smith chart:
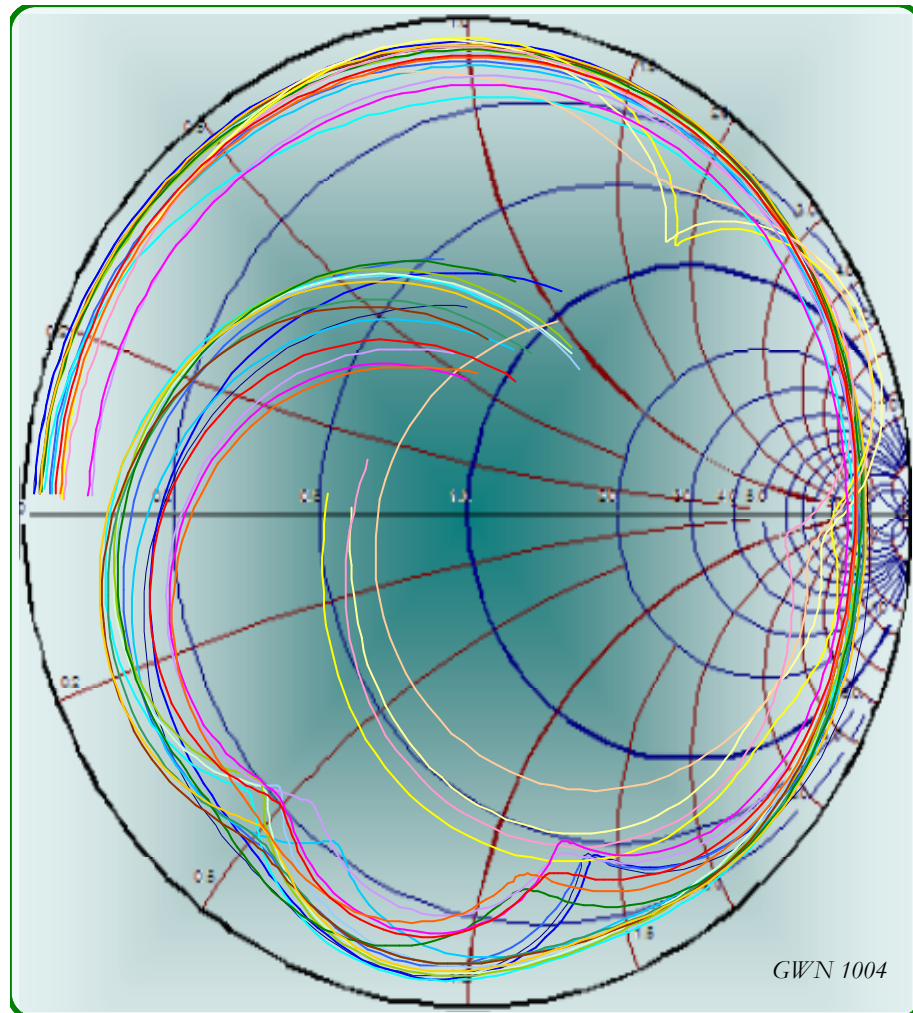

Figure 24 Short circuit response in the Smith chart

Some loss and resonances at elevated frequencies are noticeable in the Smith chart for the short circuit condition.

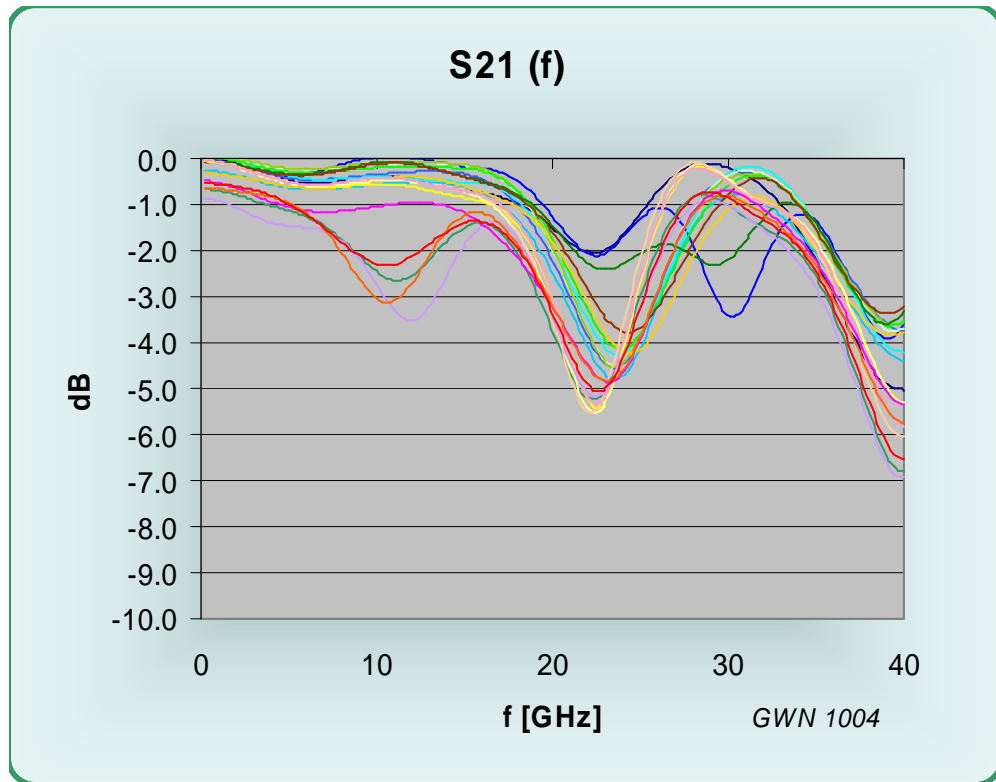An insertion loss measurement is shown below for the frequency range of 50 MHz to 40 GHz.

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Figure 25 Insertion loss S21 (f)

Insertion, like other parameters before, shows some variation, especially at frequencies above 15 GHz.   As can be seen from the statistics, there is some property deterioration after 1 million cycles.
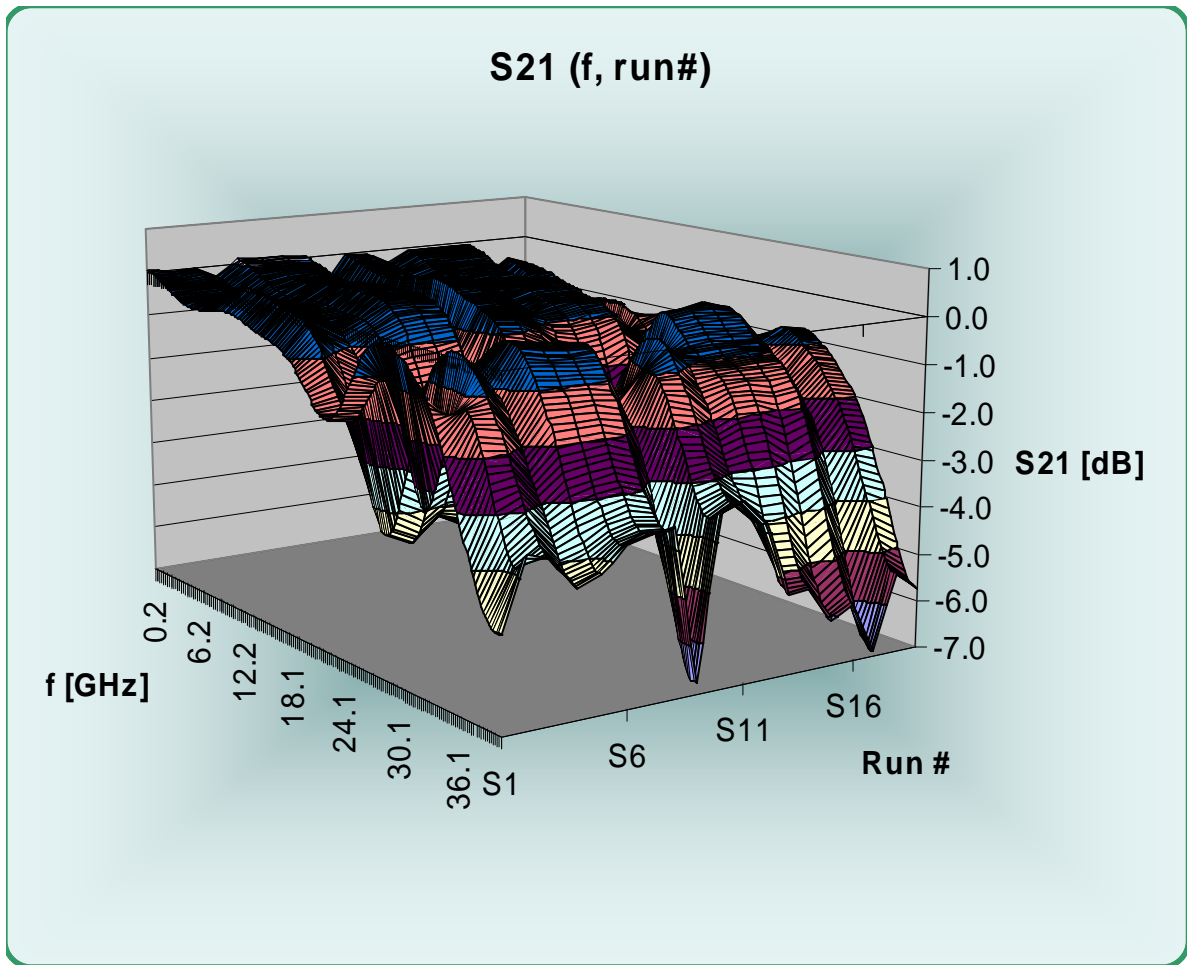
A 3D plot shows how S21 evolves with cycling:

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Figure 26 Insertion loss S21 (f) as a function of cycle #

Deviations in the datasets for each frequency point from cycle 1 to 20 are recorded as a function of frequency and also reveal this as follows:
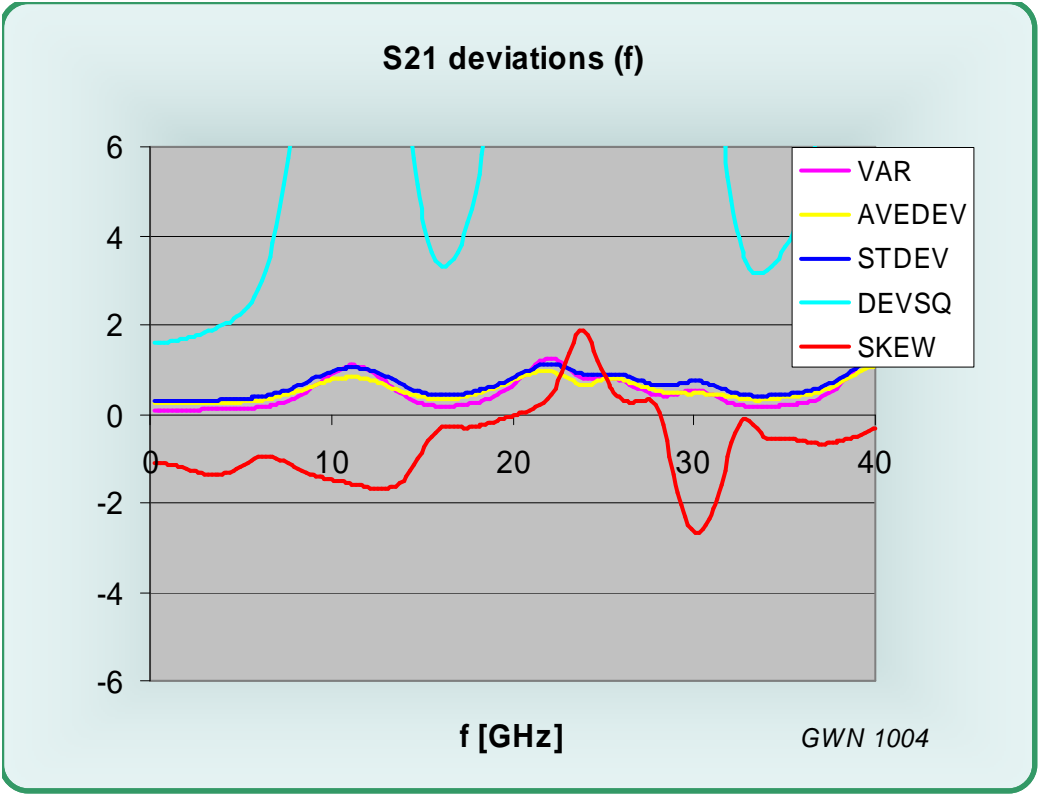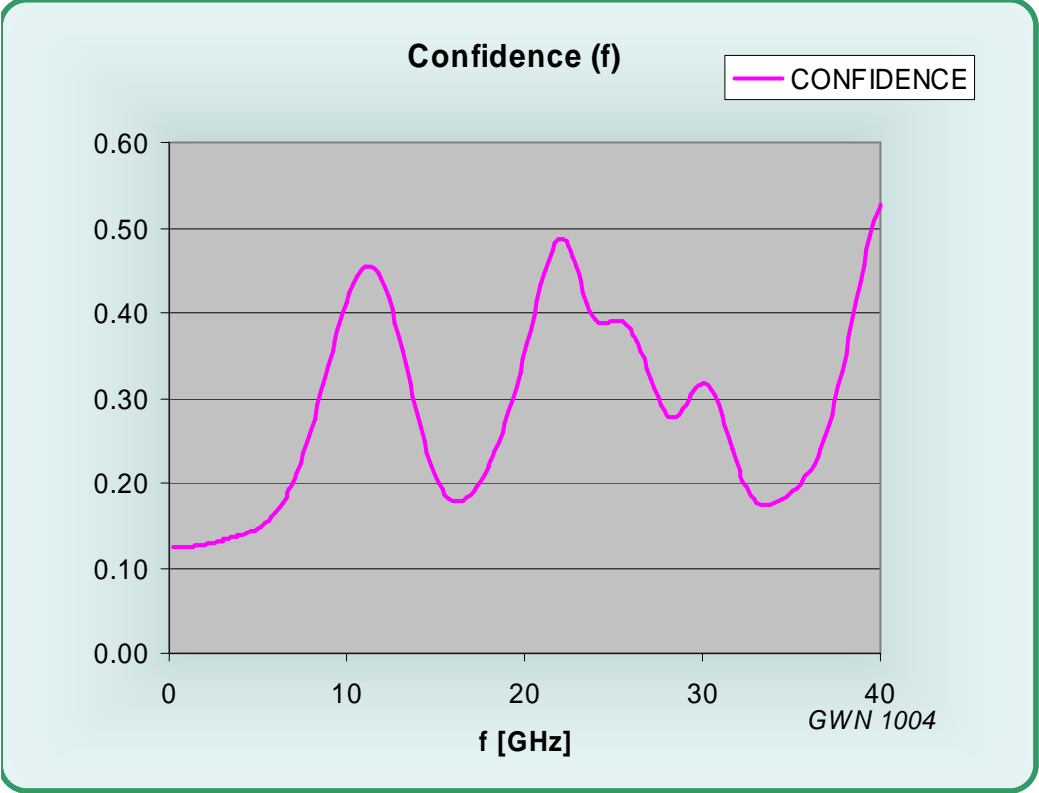
S21 deviations (f)

Legend: VAR, AVEDEV, STDEV, DEVSQ, SKEW

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Figure 27 and 28   Insertion loss S21 (f) deviations

Confidence (f)
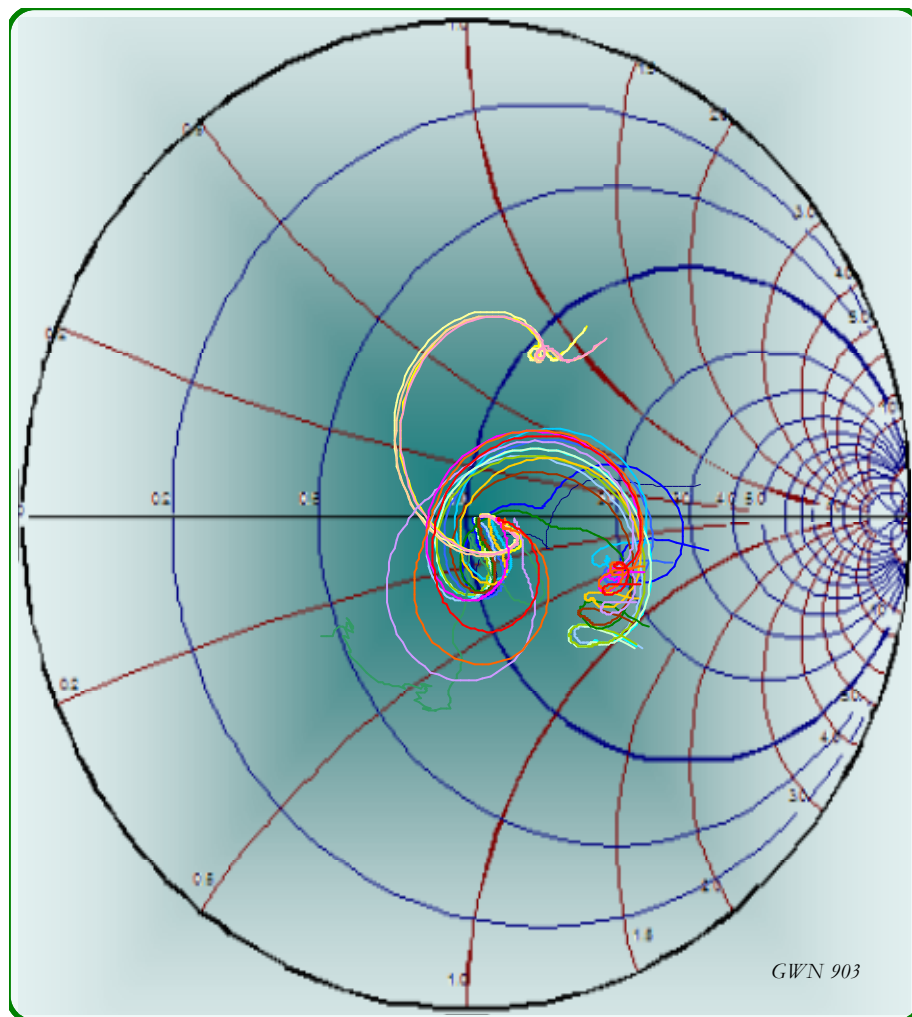
CONFIDENCE

GWN 1004

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Figure 29 Smith chart for the thru measurement into a 50 Ohm probe

The Smith chart for the thru measurements shows a reasonable match with some capacitive components toward 40 GHz. Only small resonances are present.

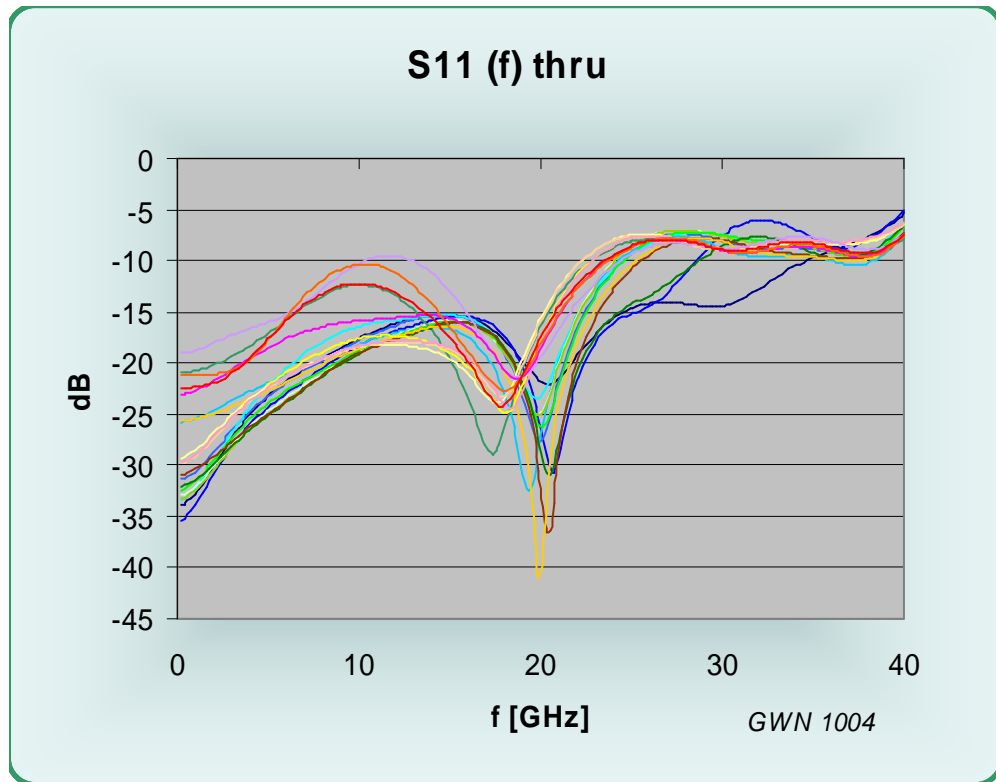*GateWave Northern, Inc.*

S11 (f) thru

GWN 1004

Figure 30 S11 magnitude (f) for the thru measurement into a 50 Ohm probe

At the highest cycle numbers some variation in performance is evident. This is also visible in a 3D plot and the statistics as seen in the graphs below. In particular, the squares of deviations show strong variations at low frequencies. This is not very meaningful, however, since even the slightest change in conditions will immediately affect the return loss at these very low signal values. In practical operation, as long as the overall S11 value is low, such changes will have little significance.
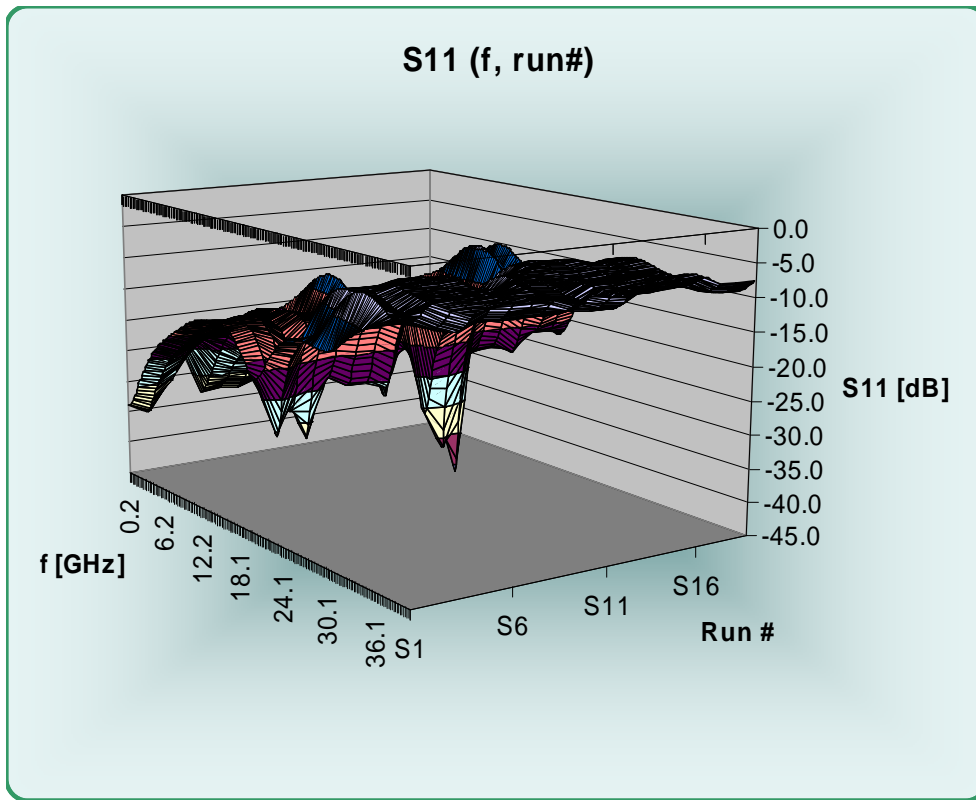
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Figure 31 S11 magnitude (f) for the thru measurement into a 50 Ohm probe
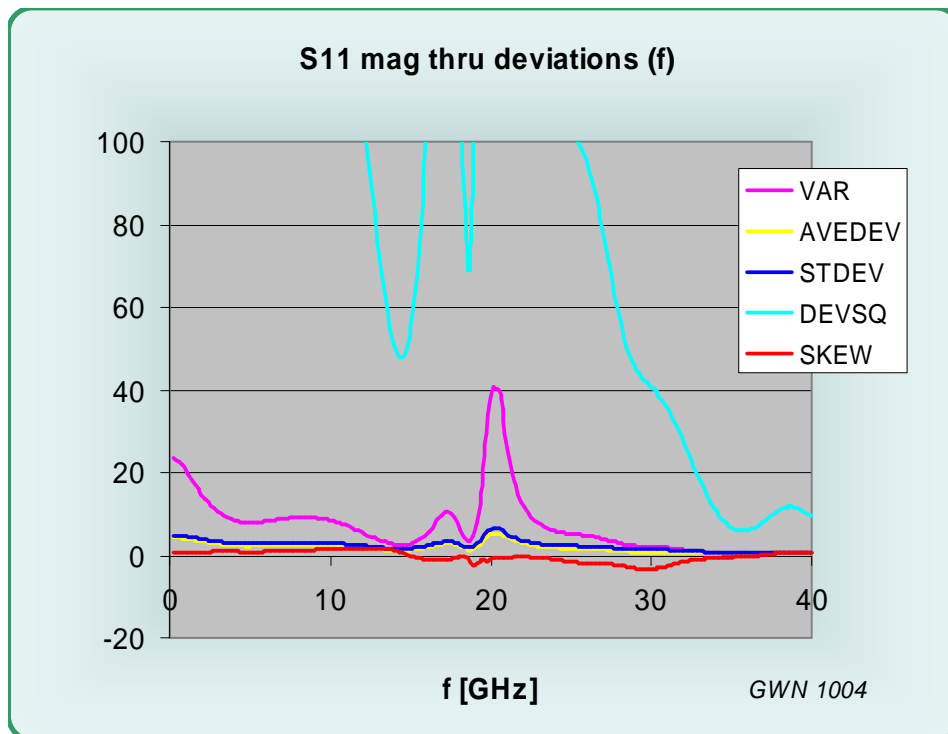
Figure 32 S11 magnitude (f) for the thru measurement into a 50 Ohm probe
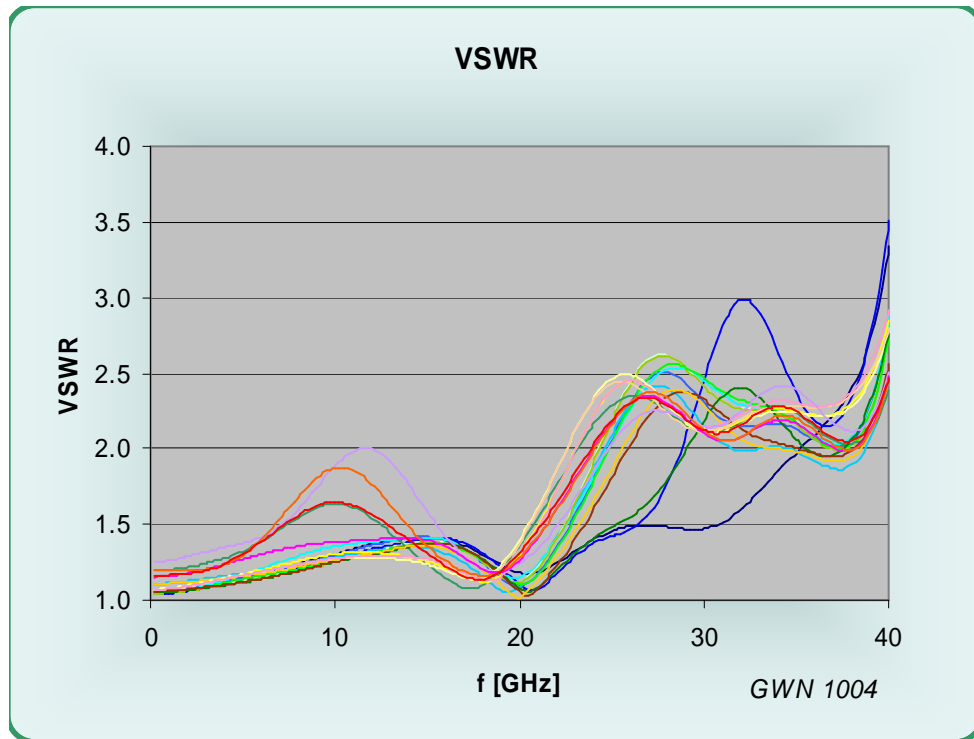
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Figure 33 Standing wave ratio VSWR (f) [1 / div.]

On average, the VSWR remains less than 2 : 1 for frequencies below 25.1 GHz.
The standard deviation for it is 2.9 GHz.

Crosstalk was measured in the G-S-S-G configuration by feeding the signal pin and
monitoring the response on an adjacent pin. Measurement results can be found in the
section on the G-S-S-G configuration.

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Measurements G-S-S-G

Time domain

Again, the time domain measurements will be presented first. A TDR reflection measurement is shown here for the thru case at port 1 to port 2:
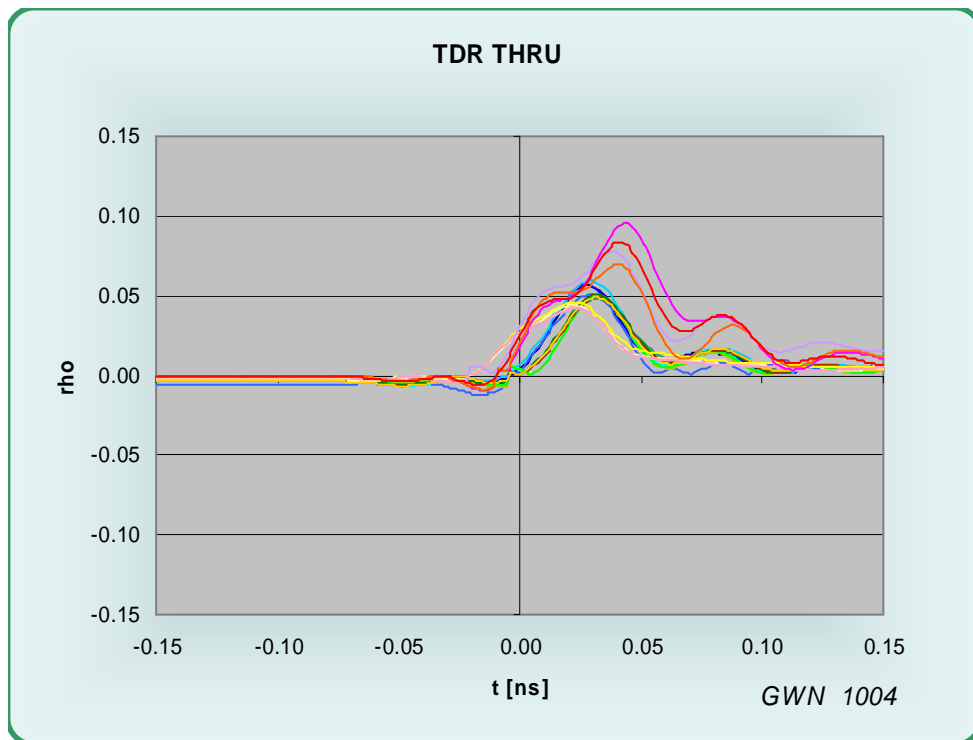

Figure 34 TDR through DUT into a terminated probe

The thru TDR response shows both inductive and capacitive responses.   The average peak corresponds to a transmission line impedance of 56.0 Ohms at a standard deviation of 1.7 Ohm. The average low point is 49.4 Ohms with a STDEV of 0.2 Ohm. The peak is higher than in the GSG case, most likely because of the fact that one of the adjacent pins is not grounded. Relatively little change occurs with cycle number.

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The TDT performance for a step propagating through the G-S-S-G pin arrangement was also recorded:
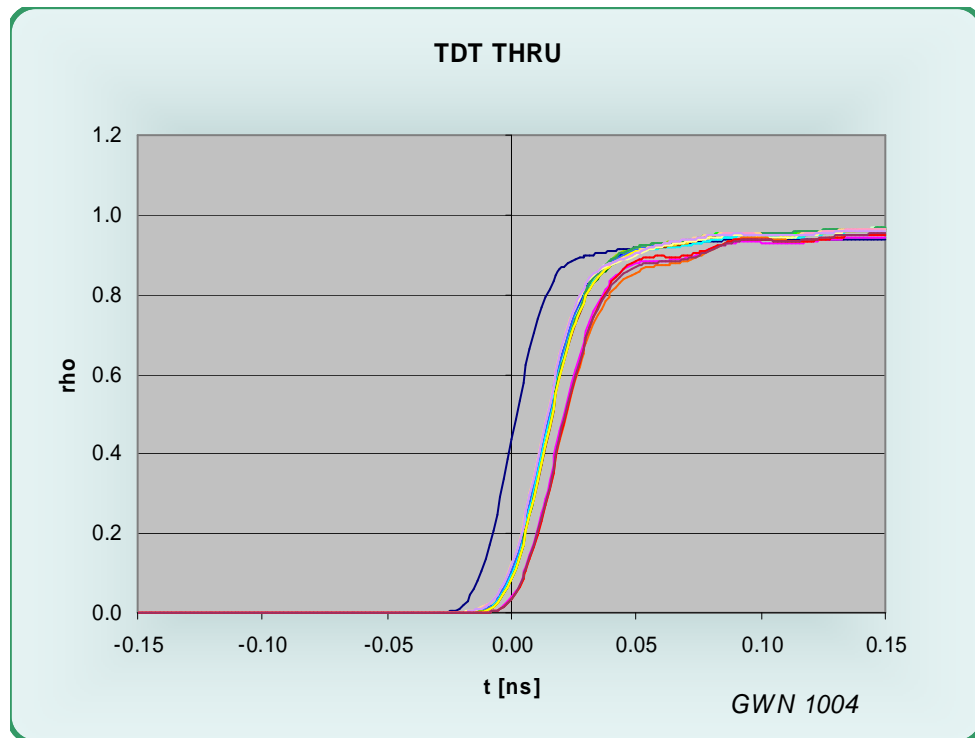

TDT THRU

GWN 1004

Figure 35 TDT measurement

The TDT measurements for transmission show some contribution to risetime from the pin array (average 10-90% RT = 37.8 ps, 1.8 ps STDEV, the system risetime is 30.0 ps). The likely source is the elevated impedance of the pin array. The average added delay at the 50% point is 14.0 ps at 2.4 ps standard deviation. The group of measurements after 1 million actuation cycles deviates noticeably from the rest of the measurements.

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Frequency domain

Network analyzer reflection measurements for the G-S-S-G case were taken with all except the pins under consideration terminated into 50 Ohms. As a result, the scattering parameters shown below were recorded for reflection and transmission through the contact array.

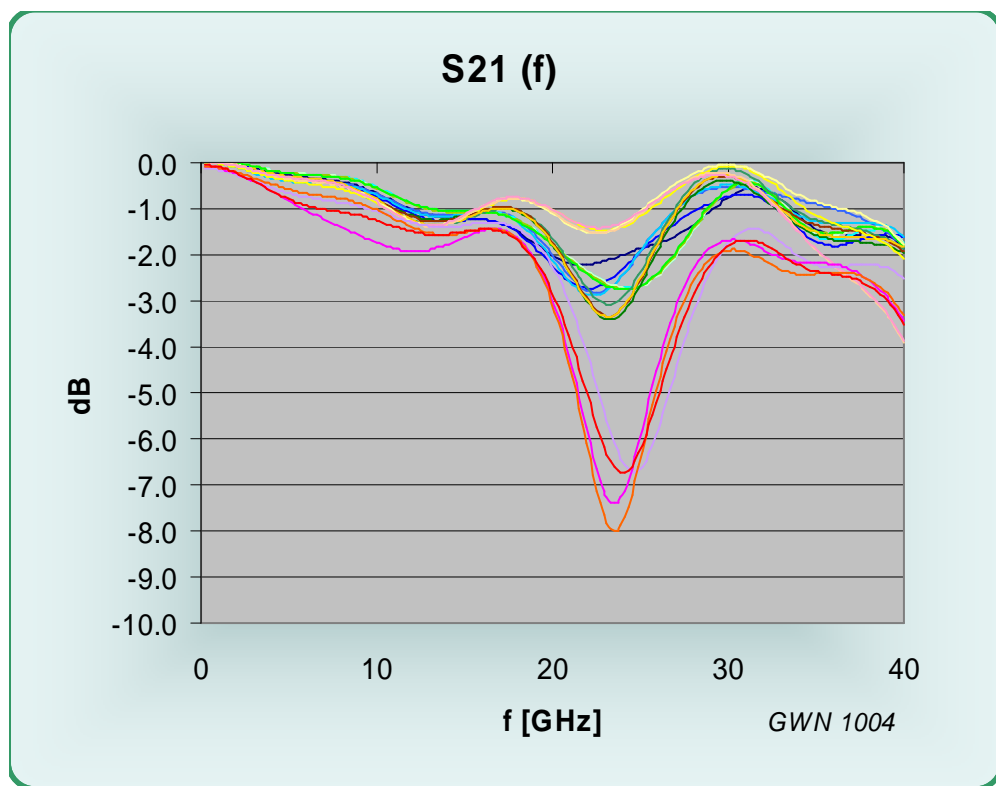First, insertion loss measurements (S21 and S12) are shown for port 1 to port 2.

Figure 36 Insertion loss S21 (f)

Insertion loss evolution at 1 million cycles shows some changes. The deviations of the datasets as a function of frequency is as follows:
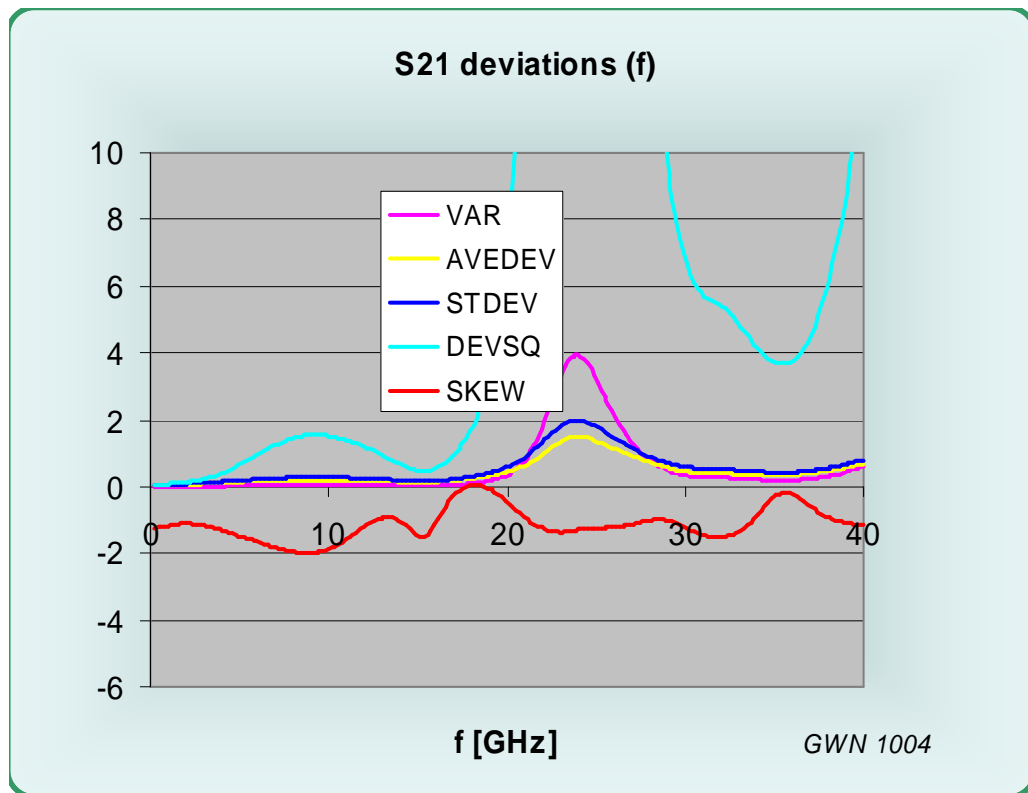
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Figure 37 Insertion loss S21 (f) deviations

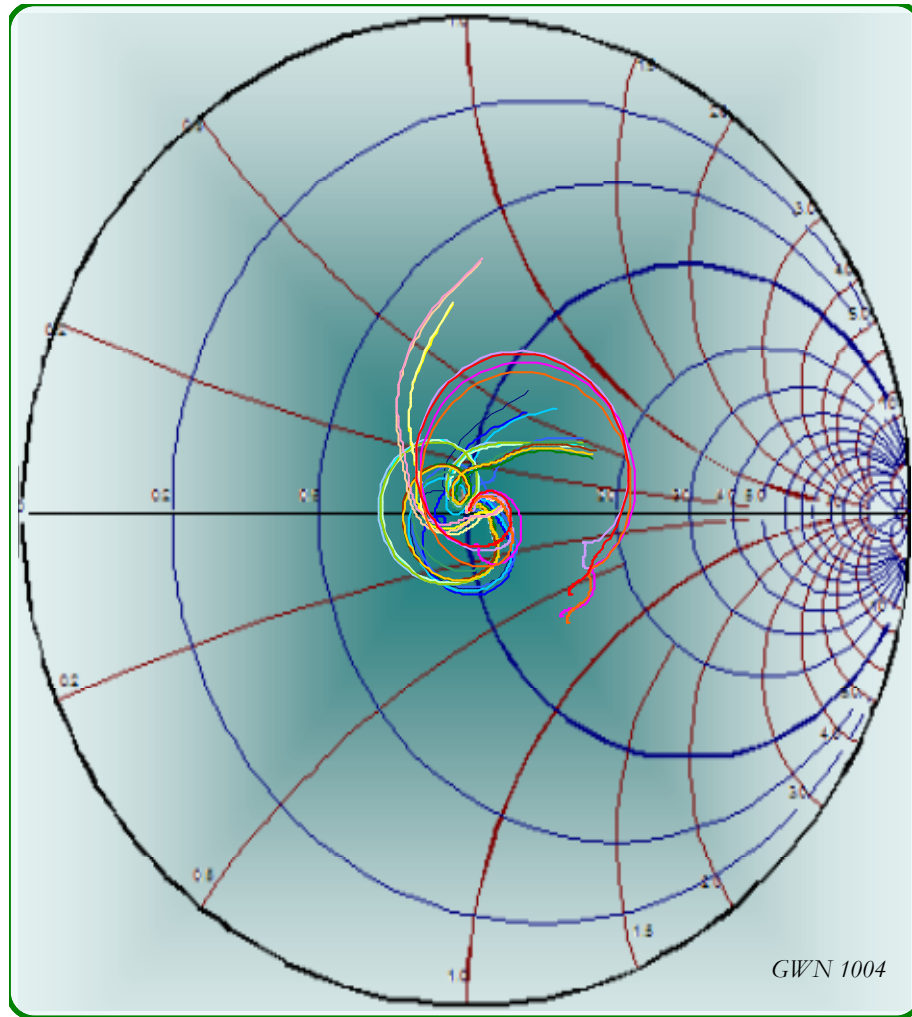The squares of deviations value rise beyond 20 GHz, signifying increased uncertainty.

Figure 38 Smith chart for the thru measurement into a 50 Ohm probe

The Smith chart for the thru measurements shows some reactive components toward 40 GHz and change at 1 million cycles
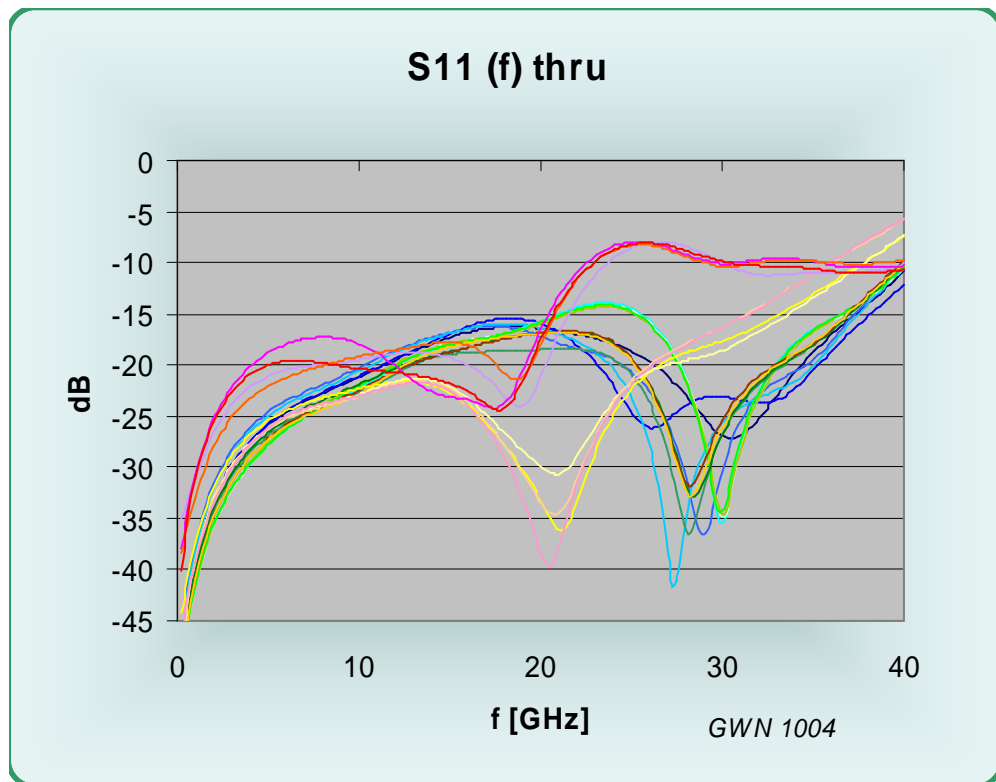
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Figure 39 S11 magnitude (f) for the thru measurements into a 50 Ohm probe

All crosstalk measurements remain low enough over the entire cycling program and do not cause concern. Variability in the results includes effects from the socket under test and the setup. It should also be kept in mind that not only the contact pins themselves participate in this response, rather than their grounded neighbors as well. Any changes in properties of these connections will also have an impact on the crosstalk. As in the case of S11 above, the squares of deviations have large values, but have these variations have little significance as long as the overall level of the crosstalk is low. At 250,000 cycles, the resonance has shifted somewhat and at 1 million cycles more significant changes occur.
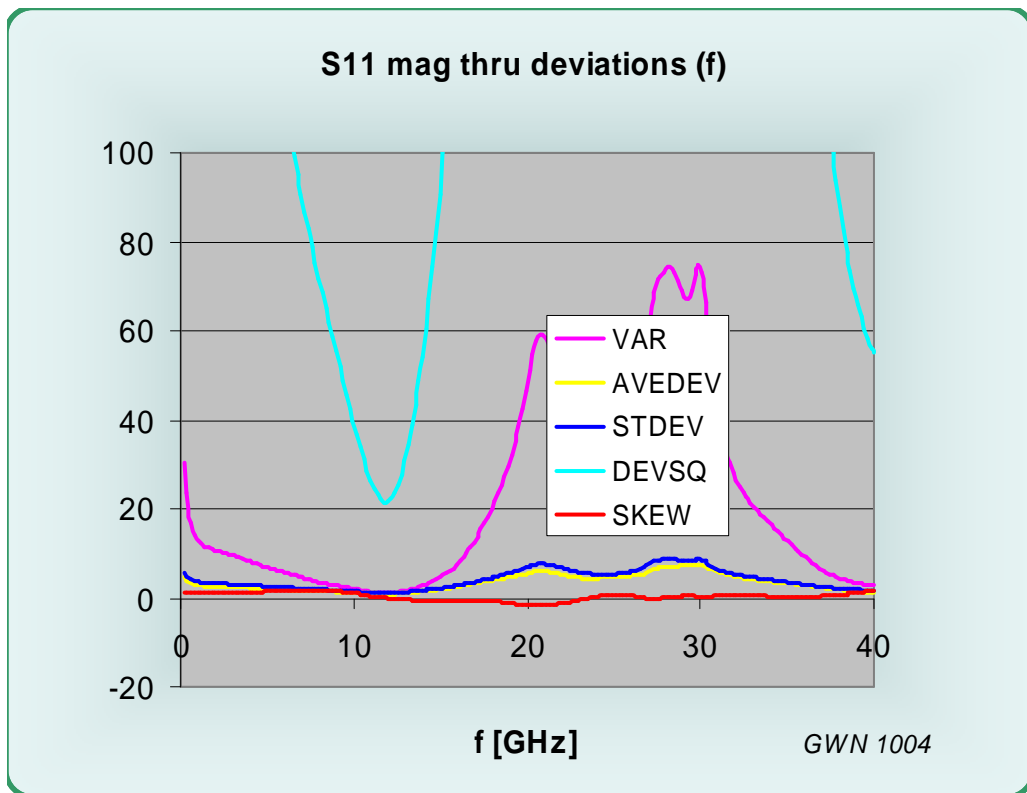
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Figure 40 S11 magnitude (f) deviations (thru measurements into 50 Ohms)
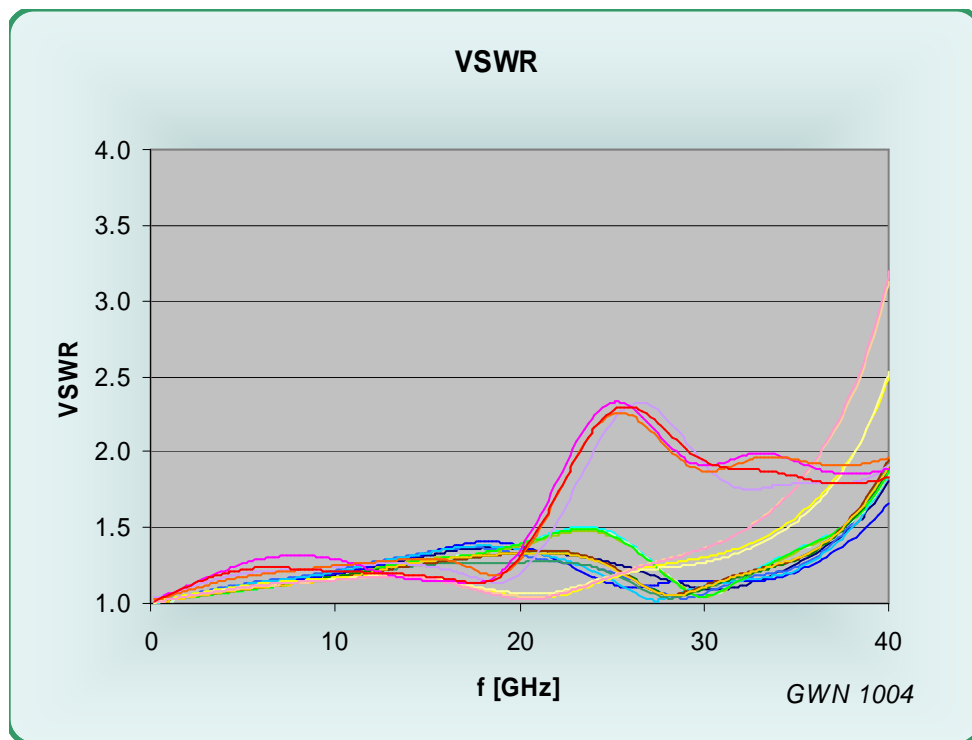
Figure 41 Standing wave ratio VSWR (f) [1 / div.]

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The VSWR remains on average below 1.2 : 1 to a frequency of 12.6 GHz (STDEV = 7.1 GHz) for S11 and on average below 2 : 1 up to 39.5 GHz (1.3 GHz STDEV; end of sweep range).

When recording the crosstalk, two cases must be considered: Forward crosstalk (S41 in the notation used here) and backward crosstalk (S31 in the notation used here):
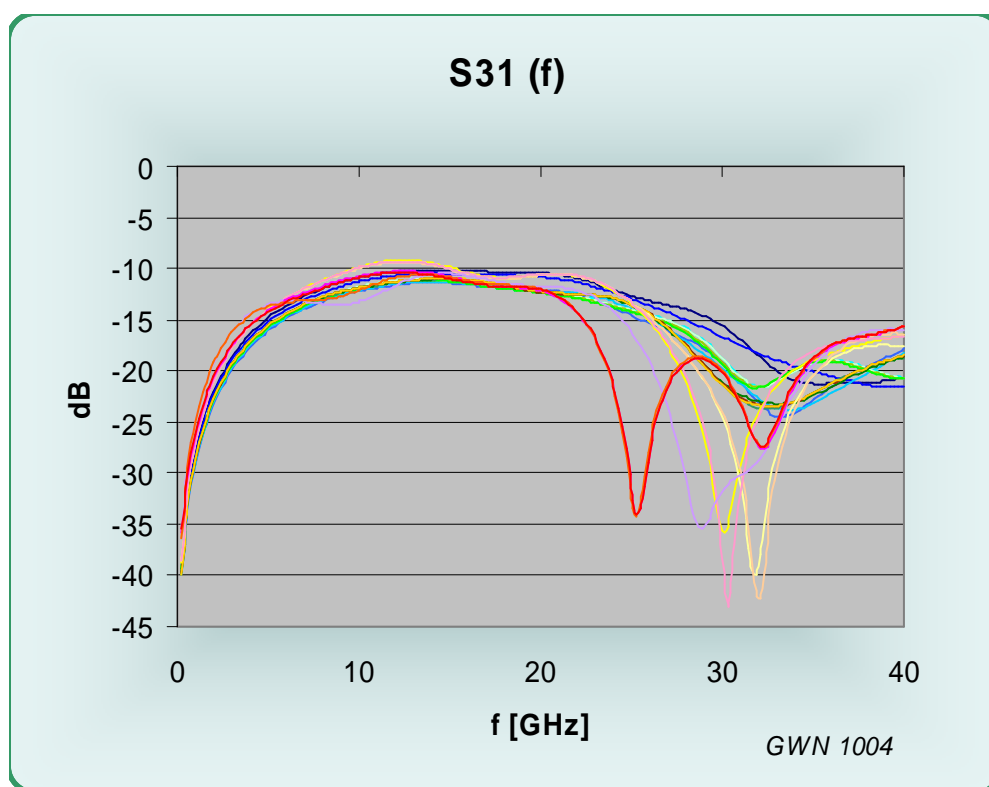
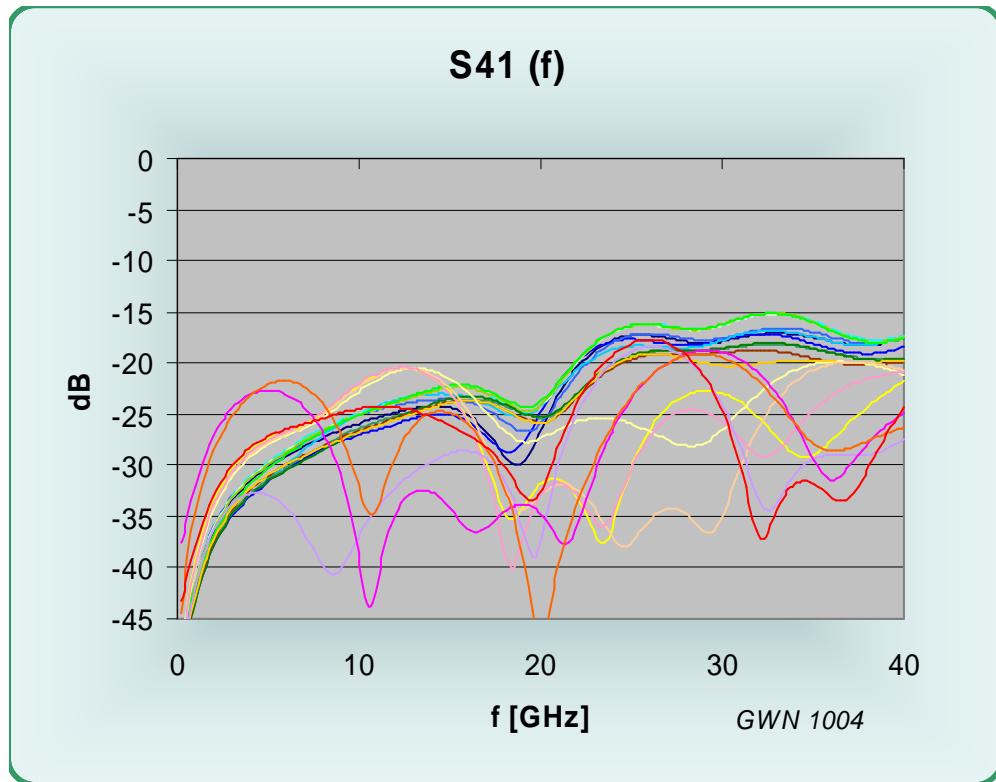Figure 42 Crosstalk as a function of frequency

Figure 43 Crosstalk as a function of frequency

The graphs show forward crosstalk from port 1 to port 4 (S41) and backward crosstalk from port 1 to the adjacent terminal (port 3, S31).   Some change in intermediate cycle numbers is evident, albeit toward improvement, not deterioration. At 1 million cycles, crosstalk at low frequencies has increased.

For the completeness the open circuit and short circuit backward crosstalk S31 are also recorded. Results are shown below. No major variations are observed throughout the cycling program.
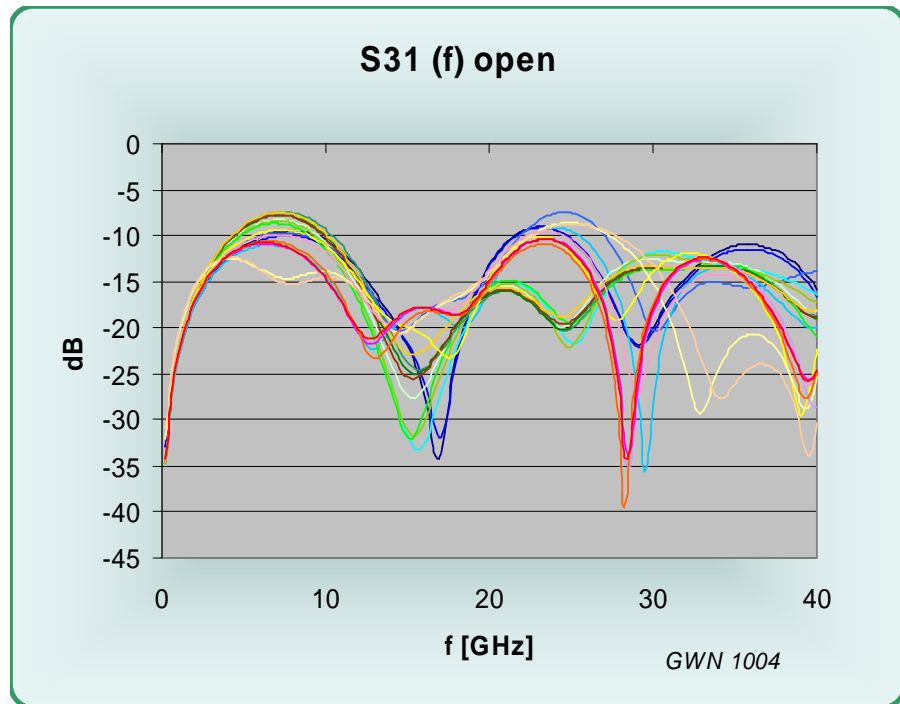
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Figure 44 Open circuit crosstalk from port 1 to port 3
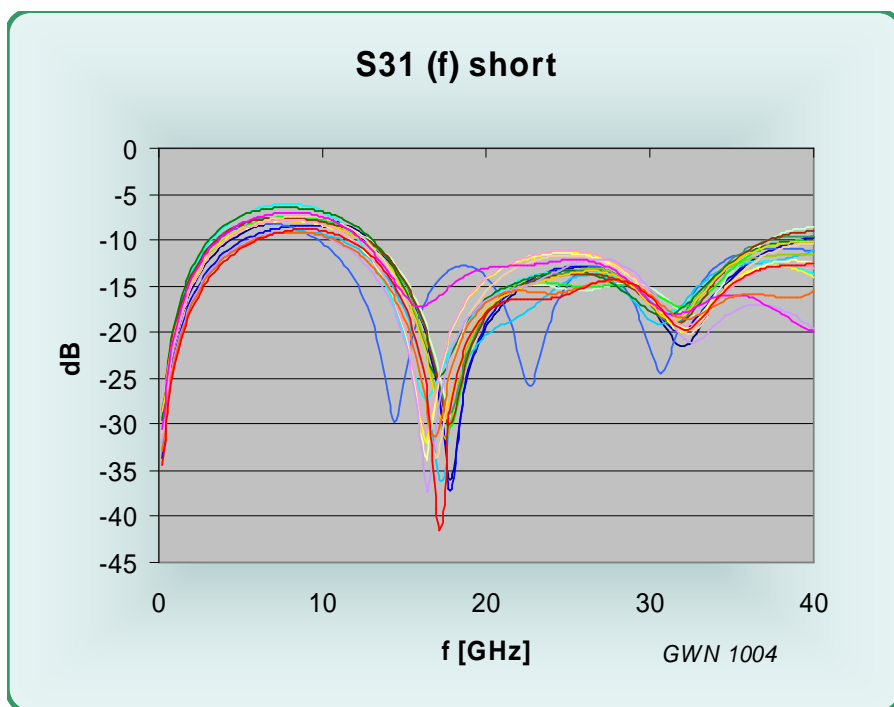
Figure 45 Short circuit crosstalk from port 1 to port 3

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Cycle chart

Shown below is a listing of the number of surrogate device insertion cycles the sockets were subjected to as a function of the sequence number. Surrogate devices were exchanged after each sequence (or 100,000 cycles, whichever is less):

1	0
2	0
3	0
4	0
5	8192
6	8192
7	8192
8	8192
9	65536
10	65536
11	65536
12	65536
13	262144
14	262144
15	262144
16	262144
17	1048576
18	1048576
19	1048576
20	1048576

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